Spectracom

MODEL 8165

WWVB DISCIPLINED OSCILLATOR

INSTRUCTION MANUAL

PLEASE NOTE OUR NEW ADDRESS

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REVISIONS, IF ANY, ARE LOCATED AT THE END OF THE MANUAL

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ERRATA DATED 1/3/95

WARRANTY

Spectracom Corporation
95 Methodist Hill Dr. Ste 500
Rochester, NY 14623

Spectracom Corporation warrants to the original purchaser each new instrument to be free from defects in material and workmanship for a period of one year after shipment. Repair or replacement, at our option, will be made when our examination indicates that defects are due to workmanship or materials. Batteries, fuses, and lamps that have given normal service are excluded from warranty coverage. All warranty returns must first be authorized by the factory.

This warranty does not apply to any of our products which have been repaired or altered by persons not authorized by Spectracom Corporation, or not in accordance with instructions furnished by us. If the instrument is defective as a result of misuse, improper repair, or abnormal conditions or operations, or if any serial number or seal has been removed or altered, the warranty is void and repairs will be billed at cost.

This warranty is in lieu of all other obligations or liabilities expressed or implied and Spectracom Corporation neither assumes nor authorizes any person to assume for them, any other liability in connection with sales of its products.

REPAIR AND MAINTENANCE

Instruments should be returned only upon prior authorization from Spectracom Corporation or its authorized sales and service representative. Warranty repair will be made upon request. Please provide the following information in order to enable us to serve you efficiently:

1. Model Number and type
2. Serial Number
3. Description of trouble
4. Conditions and hours of use

Upon receipt of this information our service department will send you service data or shipping instructions. Transportation to the factory is to be prepaid by the purchaser.

For assistance contact your nearest Spectracom sales representative.

WARRANTY REGISTRATION

Spectracom Corporation
95 Methodist Hill Dr. Ste 500
Rochester, NY 14623

Dear Customer,

Spectracom occasionally contacts customers regarding our products. We must know to whom we should send manual updates, change notices, and new product information. Because people sometimes change job assignments, we request department, mail station, and title information to ensure that correspondence in future years will reach either the user of our products or his/her supervisor. In filling out the registration, please use the title/mail station/department of the supervisor most interested in keeping the equipment and its documentation up-to-date. Thank you.

- -

Name _____ Title _____

Department _____ Mail Stop _____

Company _____ Model Number _____

Address _____ Serial No. _____

City _____ Date Installed _____

State _____ Zip _____

Telephone _____ Ext. _____

Remarks (problems, suggestions, etc.): _____

_____

_____

_____

_____

MODEL 8165

CERTIFICATE OF TRACEABILITY

Spectracom Corporation hereby certifies that its Model 8165 WWVB Disciplined Oscillator provides direct traceability to the National Institute of Standards and Technology reference frequency as transmitted by station WWVB in Fort Collins, Colorado, with a carrier frequency of 60 kHz.

Automatic verification is provided by the station-identifying phase shift of 45° that appears on the carrier signal at 10 minutes after each hour, returning to normal five minutes later. This phase shift appears as an offset of about 2.1 microseconds on a panel meter or chart recorder output.

When properly installed and maintained, the Model 8165 provides measurement accuracy and resolution as published in the equipment's instruction manual.

SPECTRACOM CORPORATION

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SECTION 1

INSTALLATION

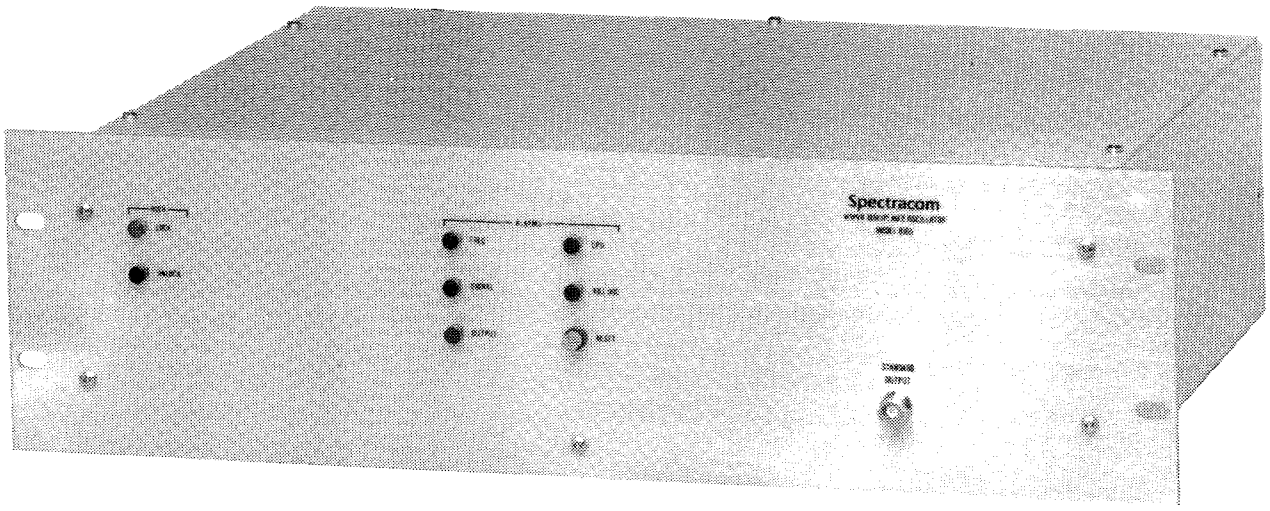


FIGURE 1-1 MODEL 8165 DISCIPLINED OSCILLATOR

INSTALLATION

1.0 INTRODUCTION

The Spectracom Model 8165 WWVB Disciplined Oscillator* is a frequency standard with accuracy directly traceable to the National Institute of Standards and Technology. The Spectracom Model 8206A Loop Antenna or Model 8208 Whip Antenna receives the 60 kHz carrier of WWVB.

The Model 8165 is continuously monitored against WWVB and kept on frequency by a microprocessor. The oscillator outputs can be used as a precise reference input for transmitters, receivers, counters, synthesizers, and other electronic equipment. Figure 1-1 shows the Model 8165 Disciplined Oscillator.

1.1 UNPACKING

Upon receipt, the carton and its contents should be carefully examined. If there is damage to the carton which results in damage to the unit, contact the carrier immediately so his representative may witness such damage. If you fail to report shipping damage immediately, you may forfeit any claim against the carrier. You should also notify Spectracom Corporation of shipping damage or shortages so that we can help you obtain a replacement or repair the damaged equipment.

Carefully open the shipping carton and remove the packing list from the envelope on the outside of the carton. Check the packing list against the contents to be sure all items have been received, including an owner's manual and ancillary kit.

Retain the carton and packing materials in the event the unit needs to be reshipped or returned to the factory.

1.2 RESHIPMENT

Use the original shipping carton if it is necessary to return the unit to the factory. If it is not available, a carton of at least 250 pound test corrugated paper with at least two inches of polyethylene foam surrounding the unit must be used. Seal the unit in a plastic bag for moisture protection and include a note stating the reason for the return. Return authorization must be obtained from Spectracom. IF THE BATTERY POWER SUPPLY IS INSTALLED, BE SURE TO SWITCH THE REAR PANEL BATTERY SWITCH TO EXT TO DISCONNECT THE BATTERY PRIOR TO SHIPPING.

* PATENT NO. 4,525,685

1.3 MODEL 8206A LOOP ANTENNA

The Model 8206A Loop Antenna reliably receives the 60 kHz WWVB transmission in field strengths of 50 μV/meter or greater. The majority of the United States exceeds 50 μV/meter as shown in Figure 1-2, Measured Field Intensity Contours. In locations having less than 50 μV/meter field strength, the Model 8207 Preamplifier is required. Refer to Section 1.7 for additional information. The equivalent electrical height of the Model 8206A is 5.0 cm.

The Model 8206A consists of a wound ferrite core surrounded by a Faraday shield which aids in noise rejection. The received signal is amplified by an internal preamplifier and output to the receiver. The preamp is powered by the receiver over the antenna coax. The antenna is packaged in a PVC housing measuring 10 inches long and 2.8 inches in diameter. The assembled antenna weight is 2.5 pounds.

The Model 8206A is a directional antenna. The tubular housing must be positioned broadside to Fort Collins, Colorado, (See Figure 1-4) and horizontal to the ground to allow maximum signal reception. No signal will be received if the tube points directly toward the transmitter site, as the antenna pattern nulls are located off the ends of the tube. The great circle map shown in Figure 1-3 is used to determine the correct antenna orientation per receiver location. The antenna position may be optimized using the AGC measurement described in Section 2.4 Signal Strength.

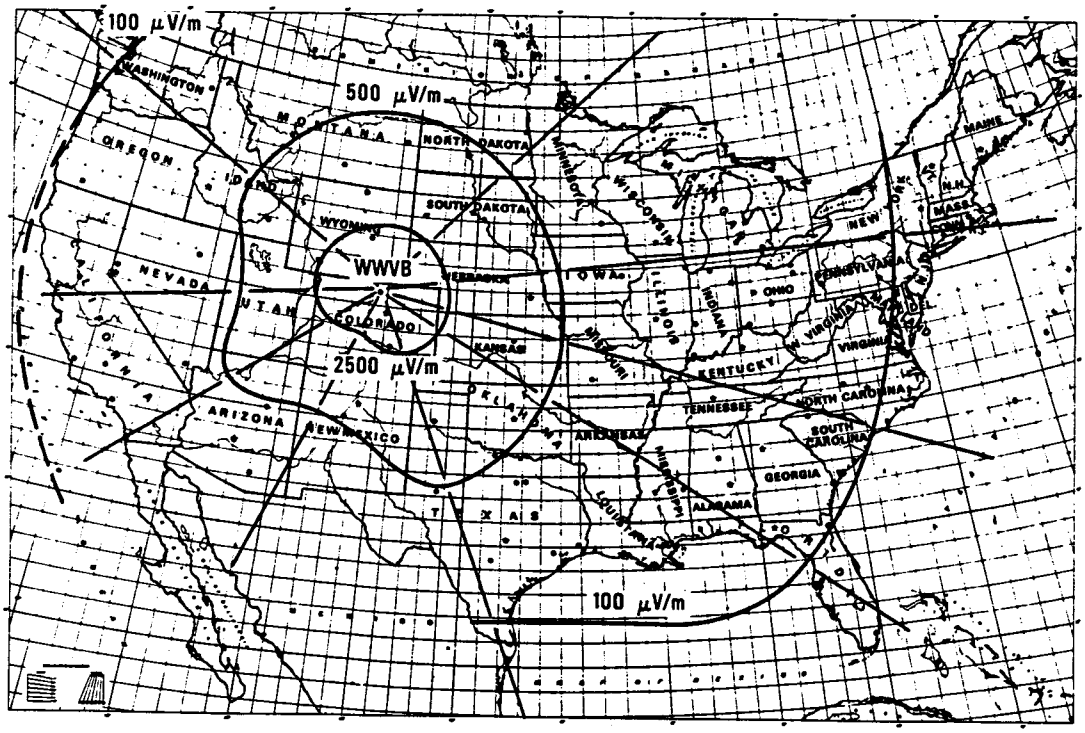
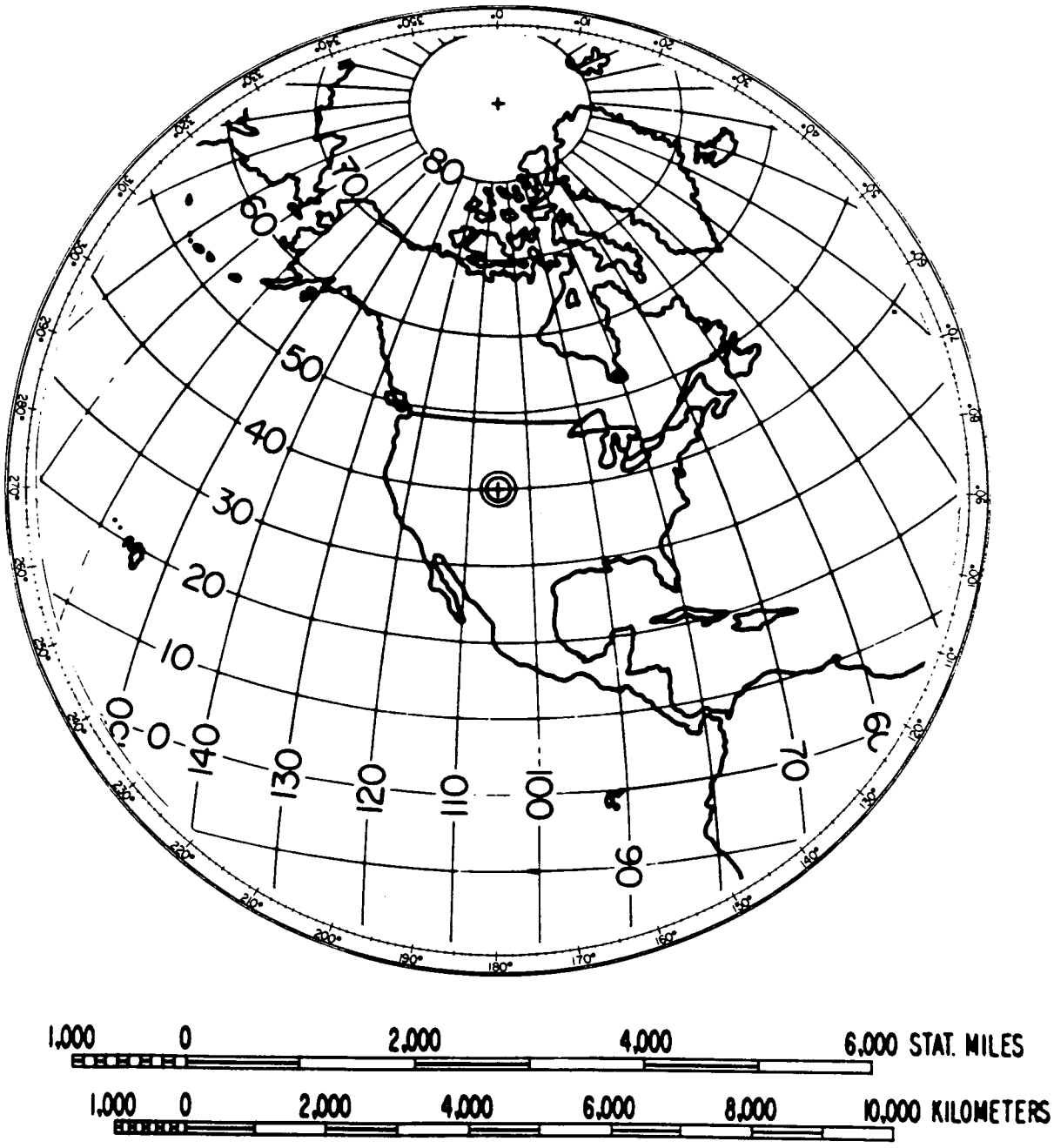


FIGURE 1-2 MEASURED FIELD INTENSITY CONTOUR WWVB @ 13 KW ERP



TO AIM ANTENNA AT FORT COLLINS, COLORADO, DETERMINE COMPASS HEADING FROM THIS MAP.

Draw a straight line from the receiver location through Fort Collins, Colo. at the center of the map. Continue until the line intersects the outer ring. The point at which the line intersects the outer ring indicates the compass heading for Fort Collins from your location.

FIGURE 1-3 GREAT CIRCLE MAP CENTERED ON FORT COLLINS, COLORADO

1.4 MODEL 8208 WHIP ANTENNA

The Model 8208 Whip Antenna provides performance equal to the Model 8206A Loop Antenna at a reduced cost. The Model 8208 may be used in field strengths of 50 μV/meter or greater. The Model 8208 contains a preamplifier housed in a weather-proof enclosure. The preamplifier is powered by the receiver over the antenna coax cable. The Model 8208 is 58.5 inches long and weighs 1.3 pounds.

1.5 ANTENNA LOCATION

The antenna should be mounted a minimum of 25 feet from the receiver to prevent regeneration. The antenna MUST NOT be positioned next to the receiver or on top of it. Doing so will make the results obtained with the equipment meaningless even though the green lock lamp on the receiver front panel may be lit.

In system installations where more than one Spectracom antenna is used, a minimum separation of 10 feet between antennas is recommended.

The antenna must be at least three feet from any steel beams, roof decking, pipes, etc., as metal will detune the antenna and can cause as much as 20 dB degradation of the signal-to-noise ratio. The antenna must not be mounted under a metal roof or inside a building with heavy steel structural supports, as these shield the antenna from the signal. Roof tops are generally good if a clear shot toward Fort Collins is available without being blocked by a large steel structure. Attics are ideal sites if the roof and rafters are not metallic. The signal-to-noise ratio will be optimized if the antenna is located as far as possible from local RF noise sources such as TV sets, or fluorescent or neon lamps that blink or sputter on and off. Any equipment containing a switching power supply is a probable cause of interference.

1.6 ANTENNA INSTALLATION

Mount the antenna where it will not be disturbed. Antenna height is not critical as the 60 kHz signal is primarily a ground wave. Holding the antenna two to three feet off the ground or rooftop is adequate. Each antenna includes a two-foot mast assembly and two hose clamps to simplify installation. A typical roof-top installation is illustrated in Figure 1-4. Spectracom offers an aluminum base, Model 8213, for installations where vent pipe mounting is not practical or desired.

NOTE: THE MODEL 8206A IS A DIRECTIONAL ANTENNA. FOLLOW THE INSTRUCTIONS FOUND ON FIGURE 1-3 TO AIM THE ANTENNA CORRECTLY.

HANDLE THE ANTENNA WITH CARE. DROPPING OR ROUGH HANDLING MAY CRACK THE FERRITE CORE, POSSIBLY DETUNING THE ANTENNA, RENDERING IT USELESS.

Spectracom recommends RG-58C/U coax for the antenna cable, though any 50-ohm coax with superior specifications may be used. The antenna coax is used to provide the antenna with its DC operating voltage and the receiver with the amplified WWVB signal. Because of low attenuation characteristics at 60 kHz and the very low power requirement of the antenna (10 mW), cable lengths up to 1,500 feet are possible if care is taken to avoid paralleling noise sources.

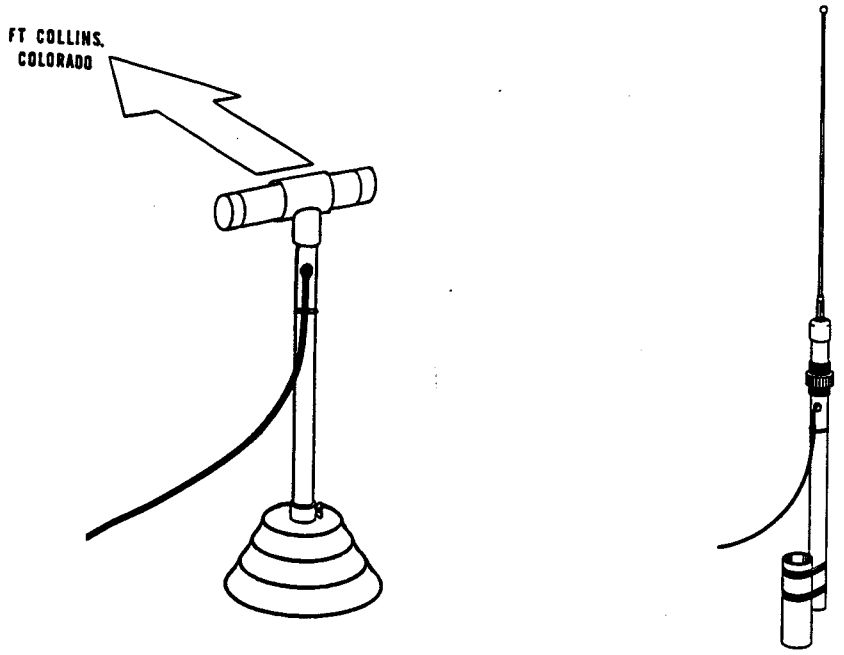


FIGURE 1-4 ANTENNA MOUNTING

1.7 MODEL 8207 PREAMPLIFIER INSTALLATION

The Spectracom Model 8207 Preamplifier is a low noise, tuned, 60 kHz line amplifier used in the antenna feed line wherever the WWVB signal strength is less than 50 μV/meter at the Model 8206 Loop Antenna or less than 0.4 μV at the receiver antenna terminal. Typical locations where the preamplifier is probably required are Hawaii, Alaska, Puerto Rico, and the Canal Zone. Figure 1-2 shows the measured average signal strength for the contiguous 48 states. Atmospheric conditions may cause short term degradation of field intensity. The Model 8207 Preamplifier provides approximately 40 dB of gain between the antenna and receiver increasing sensitivity to 4.0 nanovolts.

The preamplifier is connected in the antenna feed line with **INPUT** connected to the antenna and **OUTPUT** connected to the receiver. Because of the high gain of the system, it is recommended that the preamplifier be located at least 10 feet away from the receiver. The antenna must be least 25 feet beyond the preamplifier. Switch A1S1 of the receiver RF Amplifier must be set at its right-hand position, marked PREAMP or P, prior to equipment turn-on, to apply DC voltage to the Model 8207 on the

antenna feed line. If the preamplifier is removed from the system, the switch must be placed in the left-hand position, marked ANT or A prior to turn-on.

1.8 MATING CONNECTORS

The mating connectors for the DATA and AUX connector on the rear panel are listed below. All other connectors are BNC type.

Connector Name	Description	Spectracom Part No.	Mfr.	Mfr. Part No.
DATA	Plug, 9 position	J03309	AMP	205204-1
	Socket pins	P04001	AMP	1-66505-0
	Shell	H52090	AMP	206478-1
	The crimping tool for the pins is AMP 90302-1. The insertion/extractor tool is AMP 91067-2.			
AUX	Plug, 15 position	P01115	MOLEX	03-09-2151
	Socket pins	P01100	MOLEX	02-09-2118
	The crimping tool for the pins is MOLEX 11-01-0002. The extractor tool is MOLEX 11-03-0006. There is no insertion tool required.			
	Interfacing information is provided in Section 2.0, Operation.			

1.9 INPUT POWER

The 8165 is operated from a 115VAC $\pm$15% 60 Hz power line, 60 VA.

1.10 OPERATING ENVIRONMENT

The equipment is designed for operation over a temperature range of -30 to +50°C. Operation at temperatures outside this range may cause equipment malfunction or damage.

1.11 OPTION 11 RACK MOUNT WITH SLIDES

Option 11 allows the Model 8165 to be mounted in a 19-inch rack with slide-out capabilities. Table 1-1 lists the hardware supplied with Option 11. Verify that these items have been received. Much of the hardware supplied with this option will not be used.

QUANTITY	DESCRIPTION
1	Right hand slide assembly
1	Left hand slide assembly
2	Filler plates (not used)
2	Adjustable rear support bracket
1	Hardware Pack containing nut plates, small rear support brackets, and assorted hardware.
1	Hardware pack containing PEM nuts and #10-32 x 1/2 truss head screws
1	Hardware pack containing #10 KEP nuts and #10-32 x 3/8 pan head screws

TABLE 1-1 OPTION 11 CHECKLIST

Install Option 11 as illustrated in Figure 1-5 and as described below:

1. Remove the chassis section from the right hand slide rail assembly. The right hand assembly is designated with the letters *RH* after the manufacturer's date code label.

   Attach the chassis section to the Model 8165 using #10-32 screws. The locking tab must be towards the rear of the unit.

2. Repeat Step 1 for the left chassis section.

3. Mount the right and left stationary sections into the rack using the appropriate rear support brackets, nut plates and required hardware.

4. Insert the receiver into the rack assembly. Secure the Model 8165 to the rack using the front panel mounting holes.

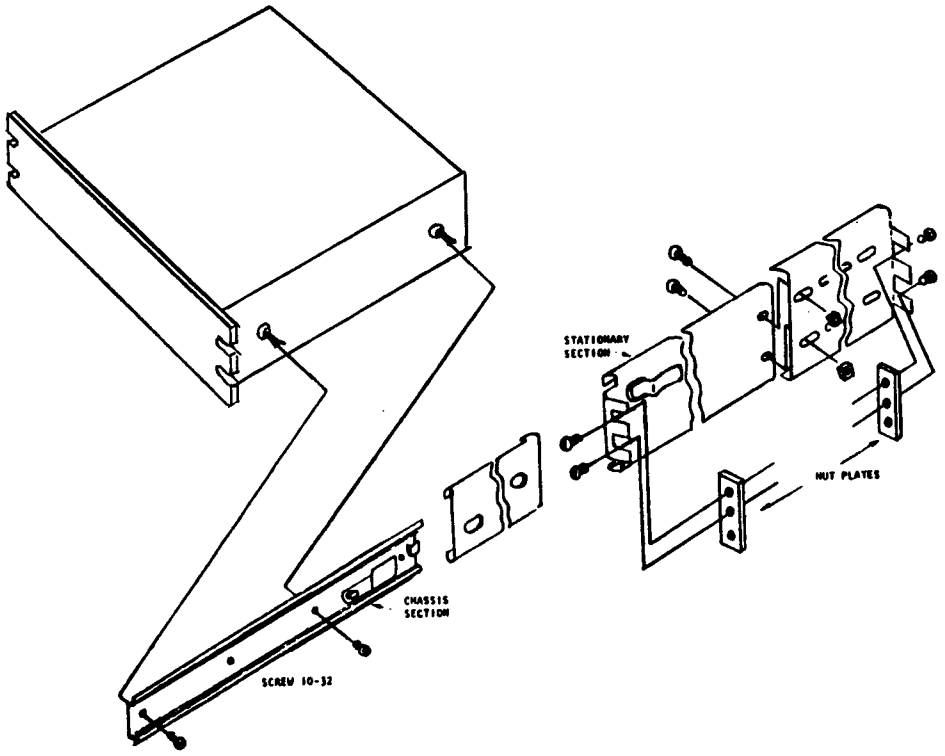


FIGURE 1-5 SLIDES, OPTION 11

MODEL 8165

SECTION 2

OPERATION

OPERATION

2.0 INTRODUCTION

This section describes the front and rear panel functions, internal switch functions, and operational information for the Model 8165 WWVB Disciplined Oscillator.

2.1 INITIAL TURN ON

Install the antenna per instructions outlined in Section 1 and slide the **OVEN DC** switch to the **INT** position. Plug the receiver into the power line and move the rear panel **POWER** toggle switch to the up position. The **CPU** lamp will briefly light then the **UNLOCK,** and **SIGNAL** lamp latch on. Once the unit phase locks to WWVB, the **LOCK** lamp will turn on and the **SIGNAL** and **UNLOCK** lamps turn off.

The receiver requires a 4-8 hour synchronization period when initially turned on. During this period of time the **FREQ** lamp may turn on. This occurs when frequency measurements indicate that the oscillator is not within 1×10^{-8} of its expected value. This condition is normal for cold oscillator startups.

The **FREQ** lamp may be reset only after the unit has frequency synchronized. To clear the lamp depress the **RESET** button.

2.2 WWVB IDENTIFICATION

WWVB identifies itself by advancing its carrier phase 45° at 10 minutes after every hour and returning the normal phase at 15 minutes after the hour. This phase shift appears as a step voltage change in the EXTERNAL PHASE METER output available at the rear panel **AUX IN/OUT** connector, Pin 11 (see 2.6.4, Pin 11).

2.3 TIME CODE OUTPUTS

Time code modulation is provided on the WWVB carrier for use in synchronizing accurate clocks and other timekeeping equipment. The modulation consists of once-per-second pulsed amplitude reductions of 10 dB, lasting either 200, 500, or 800 milliseconds. Decoding a one- minute data stream yields date, time of day, and a correction factor for converting from atomic time (Coordinated Universal Time or UTC) to celestial time (UT1). (See Figure 2-1.)

Atmospheric noise levels at 60 kHz are occasionally high, and sometimes cause false pulses to appear on the demodulated time code output. The noise levels are extremely variable, depending on factors such as season, time of day and geographical location. Noise is lower in the northern latitudes during winter daytime hours, and higher at night during the summer in southern latitudes. In U.S. coastal areas, where the WWVB signal strength is nominally 100 μV per meter, the signal-to-noise ratio

may be as high as -23 dB in a 1-kHz bandwidth. The Spectracom receiver, due to its unique synchronous detector with extremely narrow bandwidth, will stay phase locked to the WWVB carrier with signal-to-noise ratios as poor as -35 dB. Time code errors will occur on bad days, however, and error detection techniques such as those used in Spectracom's Model 8171 Synchronized Clock are necessary if the output data is to be useful.

The 10 dB reduction of the WWVB carrier is inverted in the demodulation process and appears at the output as a positive-going TTL-compatible pulse with a fan out of 2. The signal is available at pin 7 of the AUX IN/OUT connector (J8) on the rear panel, and may be used to synchronize the Model 8171 Synchronized Clock.

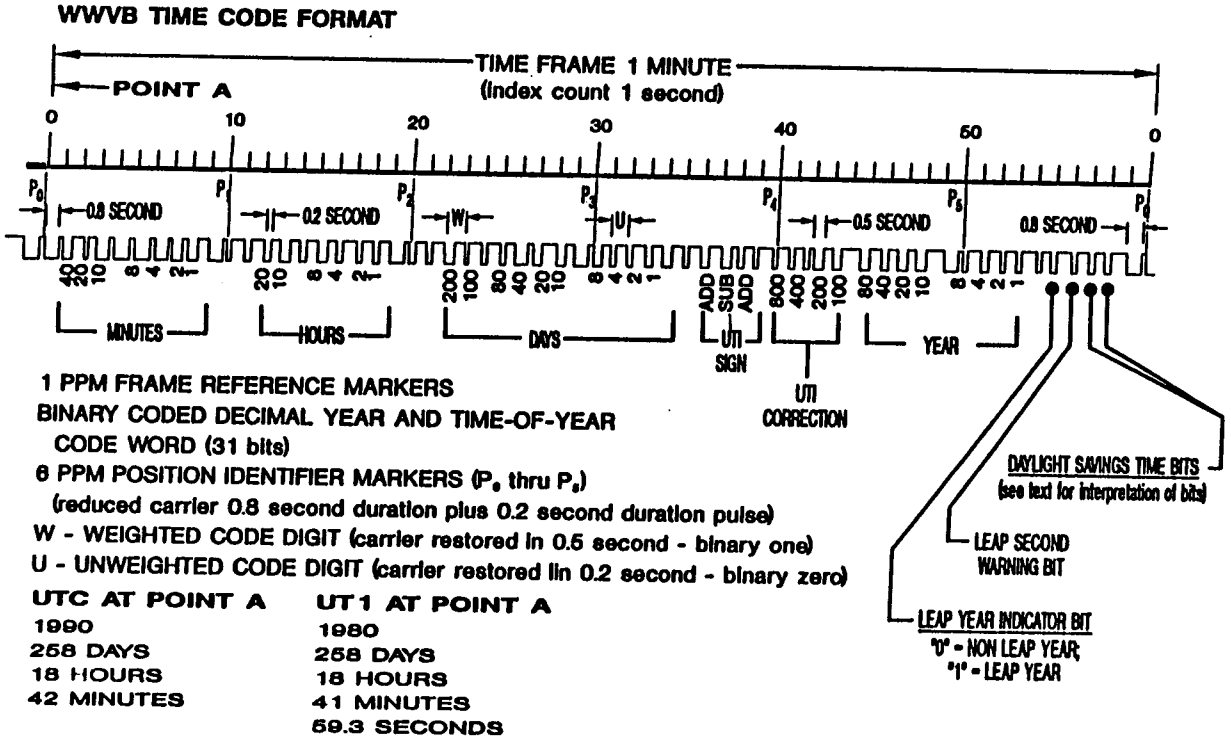


FIGURE 2-1 WWVB TIME CODE FORMAT

2.4 SIGNAL STRENGTH

The Spectracom receiver may be used to measure relative field strength of the 60-kHz signal. This measurement may be used to optimize reception by indicating the best location and orientation of the antenna.

The WWVB receiver employs synchronous AGC which responds to the 60- kHz signal only and is not affected by noise. The AGC level, therefore, provides an excellent indication of signal strength.

To measure this AGC voltage, open the cover of the receiver and locate test points TP3 and TP6 on the Receiver board A2. Place the positive lead of a DC voltmeter on TP6 (blue) and the negative lead on TP3 (orange). Refer to the receiver board assembly drawing found on page 4-11, to assist in test point location. The voltage is approximately 2.0 VDC at a field strength of 100 μV/meter using a Model 8208 Whip Antenna or a properly oriented Model 8206A Loop Antenna. The AGC voltage will increase in strong signal locations, rising to a limiting value of approximately +3.6 volts as the front end input increases.

As the signal strength decreases to the receiver phase lock threshold of about 0.2 μV, the AGC voltage decreases to about +1.0 VDC. The red **UNLOCK** panel lamp will light below this level. The AGC voltage decreases to a varying level around zero if the input signal is removed completely. As the signal is reapplied and increased, the receiver will again lock at an AGC level of approximately 1.0 volt.

The relative signal strength measurement may be used to aid antenna orientation by placing the antenna so as to maximize the AGC voltage measurement. The circuit that develops the AGC voltage has a very long time constant. A pause of 30 to 60 seconds is necessary after each move of the antenna to allow the AGC to stabilize at the new level. A few minutes of experimentation should produce optimum antenna orientation.

2.5 FRONT PANEL FUNCTIONS

Use Figure 2-2, MODEL 8165 FRONT PANEL, to locate the following.

2.5.1 UNLOCK/LOCK Lamps

The red **UNLOCK** lamp, when lit, indicates that the receiver is not locked to the WWVB carrier. This condition is usually caused by improper antenna installation (see ANTENNA LOCATION in Section 1). The green **LOCK** lamp indicates that the receiver is phase locked to WWVB.

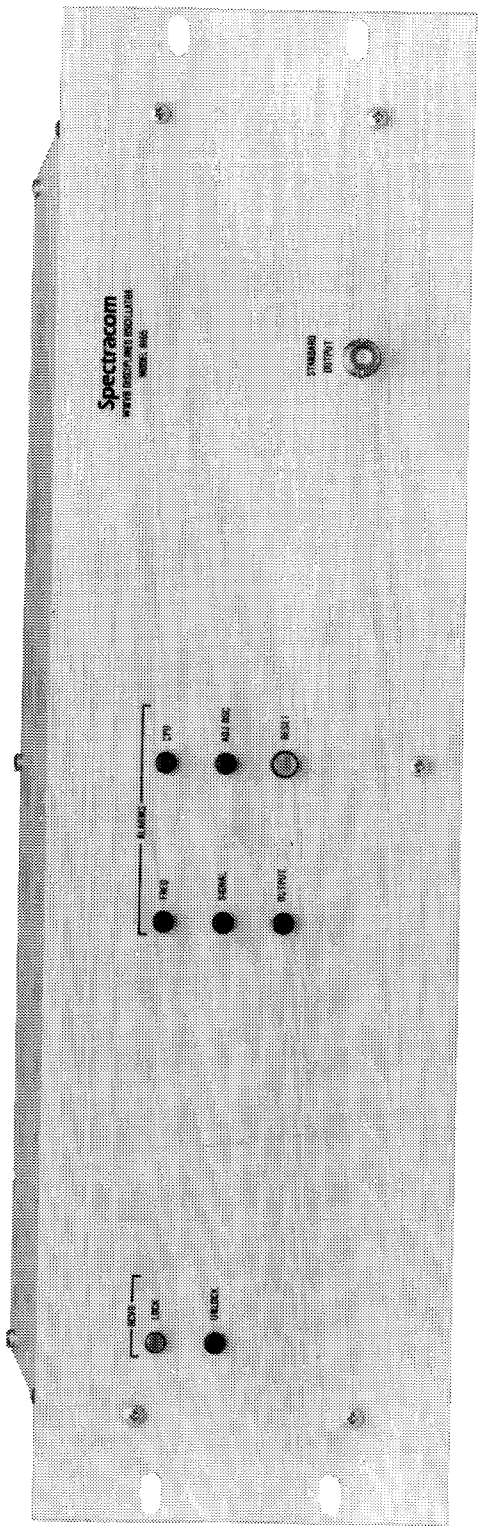


FIGURE 2-2 MODEL 8165 FRONT PANEL

2.5.2 Standard Output

This BNC connector outputs a 10 MHz signal derived from the internal standard oscillator. The output is TTL-compatible and has a 75 ohm source impedance.

2.5.3 Lamp Reset Switch

This momentary contact pushbutton extinguishes the latched alarm lamps, if the alarm condition is no longer present.

2.5.4 Alarm Lamps

FREQ - This lamp is the frequency error alarm. The lamp is latched on if subsequent measurements are off by more than $1x10^{-8}$. Once the receiver resynchronizes to within $1x10^{-8}$ of the expected frequency, the alarm may be cleared by depressing the **RESET** button. This normally takes 3-4 hours under good signal conditions. This lamp is active if the internal switch A6U1-7 **FREQ** is switched on.

SIGNAL - This lamp is the WWVB signal lamp. At power on the lamp is lit. The lamp is turned off when phase lock with the WWVB carrier is achieved. If phase lock with WWVB is lost for more than 10 hours, the lamp is latched on. The lamp is turned off by the front panel **RESET** switch.

OUTPUT - This lamp is latched on whenever the rear panel outputs vanish due to an external short circuit or reflections due to unterminated output cables. Terminate cables into 50 ohms. A Major Alarm will disable the outputs if the signature control switch is in the "ON" position, turning on the **OUTPUT** alarm lamp. Under signature control the **OUTPUT** lamp lights whenever a power failure occurs. The **RESET** switch turns the lamp off if the fault has been corrected.

CPU - The lamp is latched ON if there is a microprocessor watchdog timer failure. The front panel **RESET** switch will turn this lamp off.

ADJUST OSC - This lamp is latched ON if the 10-MHz standard oscillator requires adjustment of its coarse tuning control. The lamp is turned off by the front panel **RESET** switch.

2.6 REAR PANEL FUNCTIONS

Use Figure 2-3, 8165 REAR PANEL, to locate the following.

2.6.1 Standard Outputs

Five BNC outputs at 10.0 MHz are provided. The signal is 600 mV rms sinewave when driving a 50-ohm load. The harmonic suppression is 30 dB.

Units equipped with Option 03, Built In Distribution Amplifier, output the standard 10-MHz on a 12 VDC offset. These outputs are used to drive Spectracom Frequency Distribution Taps. Refer to the Option Section of this manual for Option 03 information.

The **STANDARD OUTPUTS** may be placed under signature control. Signature control removes the outputs whenever a Major Alarm occurs. The OUTPUT alarm lamp turns on to indicate that the rear panel outputs are not present. The STANDARD OUTPUTS are returned when the fault condition is cleared. Refer to Section 2.7.3 for additional information on signature control.

2.6.2 Alarm Outputs

The Model 8165 has two relay contact alarm outputs: the Minor Alarm and the Major Alarm. Both relays are Form C, 2A, 30 VDC contacts. The mating alarm connector is furnished in the Ancillary Kit.

The Minor Alarm is activated by the RS-422 Minor Alarm signal from the CPU board. A Minor Alarm energizes a relay, completing contact between Pins 1 and 3. Pin 2 is open. A Minor Alarm is caused by an **OUTPUT** or **ADJ OSC** alarm.

A Major Alarm is activated by the RS-422 Major Alarm signal from the CPU board. A Major Alarm de-energizes a relay, completing contact between Pins 4 and 6. Pin 5 is open. A Major Alarm is caused by a power failure or a **FREQ, SIGNAL,** or **CPU** alarm.

The alarm relays reset when the alarm condition has cleared. The front panel lamps will remain latched on until the **RESET** button has been pressed. If the alarm was caused by a CPU alarm, neither the Major Alarm relay or CPU lamp will clear until the **RESET** button has been pressed.

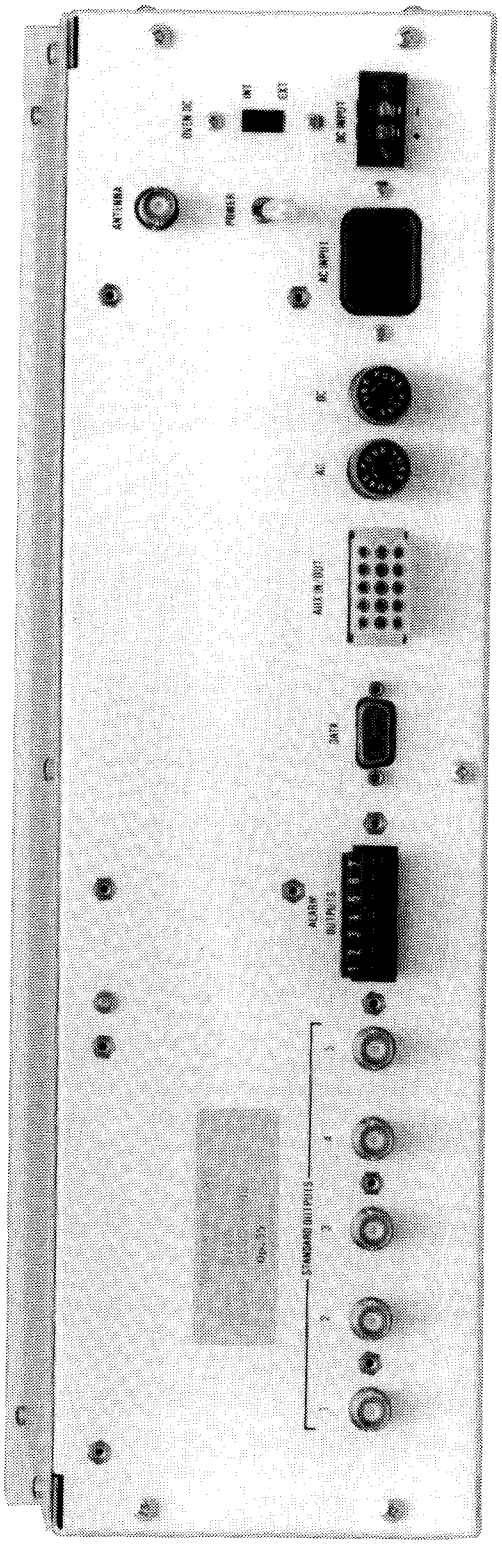


FIGURE 2-3 MODEL 8165 REAR PANEL

2.6.3 Oven DC INT/EXT Switch

This switch selects the source of the oscillator standby supply. The standby supply powers the standard oscillator whenever AC power is lost. This avoids settling and retrace problems when the AC power returns.

When this switch is in the **INT** position an internal battery pack is selected as the standby supply. The batteries are continuously float-charged whenever line power is connected to the unit. The battery pack contains sealed lead-acid cells that require no maintenance. The battery pack provides a minimum of 36 hours of standby operation and is standard in the Model 8165. The battery pack is not present in units with DC Input Options, 52, 53, 54, or 55.

NOTE: THE INTERNAL BATTERY HAS BEEN DISCONNECTED FOR SHIPMENT BY PLACING THE **OVEN DC** SWITCH IN THE **EXT** POSITION. TO RECONNECT THE BATTERY, RETURN THE SWITCH TO THE **INT** POSITION.

If the unit is disconnected from AC power for more than 36 hours or if the unit is returned to the factory for repair, place the switch in the **EXT** position.

In the **EXT** position the switch selects an external battery as a standby supply. The external battery connections are made at the rear panel **AUX IN/OUT** connector. See Pin 3 of the **AUX IN/OUT** description for battery recommendations.

2.6.4 AUX IN/OUT (J8)

Auxiliary and remote functions of the receiver are available at this 15-pin connector. Use Figure 2-4, AUX IN/OUT (J8) VIEWED FROM THE REAR OF THE UNIT, to locate the pins. The mating connector and pins are furnished in the Ancillary Kit.

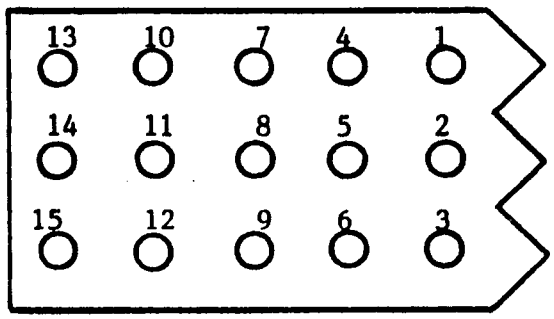


FIGURE 2-4 AUX IN/OUT (J8), VIEWED FROM THE REAR OF THE UNIT

PIN 1 - (+) MINOR ALARM - This lead is positive relative to PIN 2 when the function is asserted. The Minor Alarm is asserted whenever an Output Fault or Adjust Oscillator Alarm occurs. Twisted pair should be used for PIN 1 and PIN 2.

PIN 2 - (-) MINOR ALARM - This lead is negative relative to PIN 1 when the function is asserted.

PIN 3 - EXTERNAL BATTERY INPUT - For continuous oven and oscillator operation in the event of power failure, an external battery can be connected here. The battery will be float-charged whenever line power is on. The maximum charge rate is 250 mA. Recommended battery type is sealed lead-acid, 24 VDC, 1-2 A-H or greater capacity. The **OVEN DC** switch must be in the EXT position.

PIN 4 - TIME CODE OUTPUT GROUND

PIN 5 - PHASE LOCK OUTPUT - Used for monitoring of receiver phase lock condition. This pin will be ground when the unit is unlocked, and +5 VDC behind 3.3K ohms when the unit is locked.

PIN 6 - EXTERNAL BATTERY INPUT GROUND

PIN 7 - TIME CODE OUTPUT - Logic high is +5 VDC behind 3.3K ohms, logic low is ground.

PIN 8 - (+) MAJOR ALARM - This lead is positive relative to PIN 9 when the function is asserted. A twisted pair should be used for PINs 8 and 9. The signal returns to normal when the alarm condition is cleared. A Major Alarm is asserted whenever the CPU, Signal or Frequency alarms occur.

PIN 9 - (-) MAJOR ALARM - This lead is negative relative to PIN 8 when the function is asserted. The signal returns to normal when the alarm condition is cleared.

PIN 10 - MAJOR ALARM GROUND - The external cable for PIN 8 and PIN 9 should be a twisted pair. This ground is reserved for the ground shield of this cable.

PIN 11 - EXTERNAL PHASE METER - This output may be used to operate a 0-1mA meter or chart recorder to compare the phase relationship between the frequency standard and the NIST phase- locked signal. Full scale represents 50 microseconds of relative time.

PIN 12 - EXTERNAL METER GROUND

PIN 13 - 10 MHZ PHASE LOCKED OUTPUT - TTL compatible, positive rectangular pulses, 100 ohm source impedance. This signal is from the NIST VCXO and will have short term jitter.

PIN 14 - 10 MHZ PHASE LOCKED OUTPUT GROUND.

PIN 15 - GROUND

2.6.5 AC Input

The standard Model 8165 is AC powered. The detachable line cord (supplied) is connected between the AC INPUT jack and a 115 VAC receptacle.

2.6.6 AC Fuse

This is the main power fuse for the unit. When operating this unit at 115 VAC use a 3/4 Amp fuse. Units equipped with Option 03 use a 1.25 Amp fuse. An appropriately sized spare fuse is supplied in the ancillary kit.

2.6.7 Power Switch

This locking toggle switch applies power to the unit.

2.6.8 DC Fuse

On all AC powered units this fuse protects the oscillator power supply. For a standard unit a 3/8 Amp fuse is used. Option 55, -24 Volt Oven Backup, requires a 1 Amp fuse. For DC input Options 52, 53, or 54, this is the main power fuse for the unit. Units equipped with Options 52, 53, or 54 require a 4 Amp fuse. An appropriately sized spare fuse is furnished in the ancillary kit.

2.6.9 DC Input

This 2-position terminal block is used for external DC power options. Be certain to observe the connectors polarity markings.

2.6.10 Data

This connector is Series D, 9-pin receptacle. The pin locations are shown in Figure 2-5. The serial channel transmits/receives an asynchronous frame that consists of a start bit, 7 data bits, a mark bit, and a stop bit. Baud rate is dip switch selectable. Table 2-1 lists baud rates and the corresponding switch settings. Refer to Section 2.9 for receiver printouts and commands.

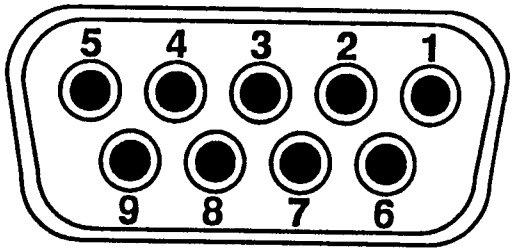


FIGURE 2-5 DATA CONNECTOR

PIN 4 SERIN	This is an RS-232C signal. Serial ASCII characters are input via this pin.
PIN 5 SEROUT	This is an RS-232C signal. Serial ASCII characters are output via this pin.
PIN 7 ON-TIME	This is a TTL-compatible 1-Hz square wave derived from the standard 10-MHz oscillator.
PIN 9 GND	Signal ground

2.6.11 Antenna

This BNC connector is the antenna input to the receiver. The antenna receives its operational power from this connector. This connector outputs 12 VDC and is short-circuit protected.

2.7 INTERNAL SWITCHES

There are two 8-position DIP switches located on printed circuit board 018101 (A6). These switches control baud rate, offset steps, and test functions. The signature control switch found on the output board (A4) enables or disables the signature control feature. The antenna power switch found on the RF amplifier board (A1) allows additional current for the Model 8207 preamplifier.

The internal switches are set as indicated below when the unit is shipped from the factory:

A6U1-1	Spare	OFF	A6U18-1	Auto Reset	OFF
U1-2	DA One	OFF	U18-2	Spare C4	OFF
U1-3	DA Zero	OFF	U18-3	Spare C3	OFF
U1-4	GATE-10	OFF	U18-4	Spare C2	OFF
U1-5	Lamp	OFF	U18-5	Spare C1	OFF
U1-6	Test	OFF	U18-6	Baud 2	ON
U1-7	Freq	ON	U18-7	Baud 1	ON
U1-8	Phase	OFF	U18-8	Baud 0	OFF

A4SW1	Signature Control OFF
A1SW1	Antenna System Power - Antenna Only

2.7.1 Switch A6U1

Plus or Minus Offset - Spare A6U1-1: This switch controls the direction of the selected frequency offset. The offset is positive when the switch is ON and negative when OFF.

Minimum Frequency - DA ONE A6U1-2: When the TEST switch is ON and DA ONE switch is ON the output of the D/A converter is all 1's. This adjusts the 10-MHz standard to its minimum value. This switch is only used during the frequency range adjustment procedure.

Maximum Frequency - DA ZERO A6U1-3: When the TEST switch is on and DA Zero switch in ON the output of the D/A converter is all zeros. This adjusts the 10-MHz standard to its maximum value and is used during the frequency range adjustment procedure.

10-Second Measurement Gate - GATE10 A6U1-4: With the TEST switch ON and the GATE10 switch ON, the measurement gate time is changed from 1000 seconds to 10 seconds. This switch is used during the frequency range adjustment procedure of the 10-MHz standard oscillator.

Lamp Test - LAMP A6U1-5: With the TEST switch ON the Lamp Test switch will turn on the alarm lamps.

Enable Test Switch - TEST A6U1-6: When this switch is ON it enables test switches U1-2 through U1-5. For normal operation it should be placed in the OFF position.

Enable Frequency Correction - FREQ A6U1-7: When this switch is in the ON position, the 10-MHz standard oscillator is automatically kept on frequency.

Enable Phase Correction - PHASE A6U1-8: When this switch is ON the accumulated time error of the standard 10-MHz oscillator is measured by comparing the oscillator output with the received time code. As time error accumulates, small corrections slew the oscillator to make up for lost or gained time. This function is not used with the Model 8165 and should be in the OFF position.

2.7.2 Switch A6U18

Auto Reset A6U18-1: Not used on the Model 8165. This switch should be in the OFF position.

Spare C4, Spare C3, Spare C2, Spare C1 - A6U18-2,3,4,5: These switches enter the binary equivalent of the frequency offset channel selected. If no offset of the 10-MHz output is required, turn these switches to the **OFF** position. Table 2-2, FREQUENCY OFFSETS, list the offsets for each switch setting.

Baud 2, Baud 1, Baud 0 - A6U18-6,7,8: These switches select the baud rate in/out of the DATA connector on the rear panel. The bit rate switch coding is shown in Table 2-1, BIT RATE.

TABLE 2-1 BIT RATE

Baud Rate	A6U18-6 Baud 2	-7 Baud 1	-8 Baud 0
300	1	1	0
600	1	0	1
1200	1	0	0
2400	0	1	1
4800	0	1	0
9600	0	0	1

2.7.3 Switch A4SW1 - Signature Control

The Model 8165 is shipped from the factory with the signature control feature disabled. Signature control when enabled removes the five rear panel standard outputs whenever a Major Alarm occurs. A Major Alarm is asserted by a frequency, signal, or CPU alarm. The output alarm lamp latches on whenever the outputs are removed. The outputs are returned when the fault condition causing the major alarm is cleared.

The signature control feature may be enabled by placing switch A4SW1 in the "ON" position. Figure 2-6 shows the location of the signature control switch.

Switch SW1- ON - Signature Control ENABLED. A Major Alarm removes outputs.
Switch SW1- OFF- Signature Control DISABLED. Alarms DO NOT remove outputs.

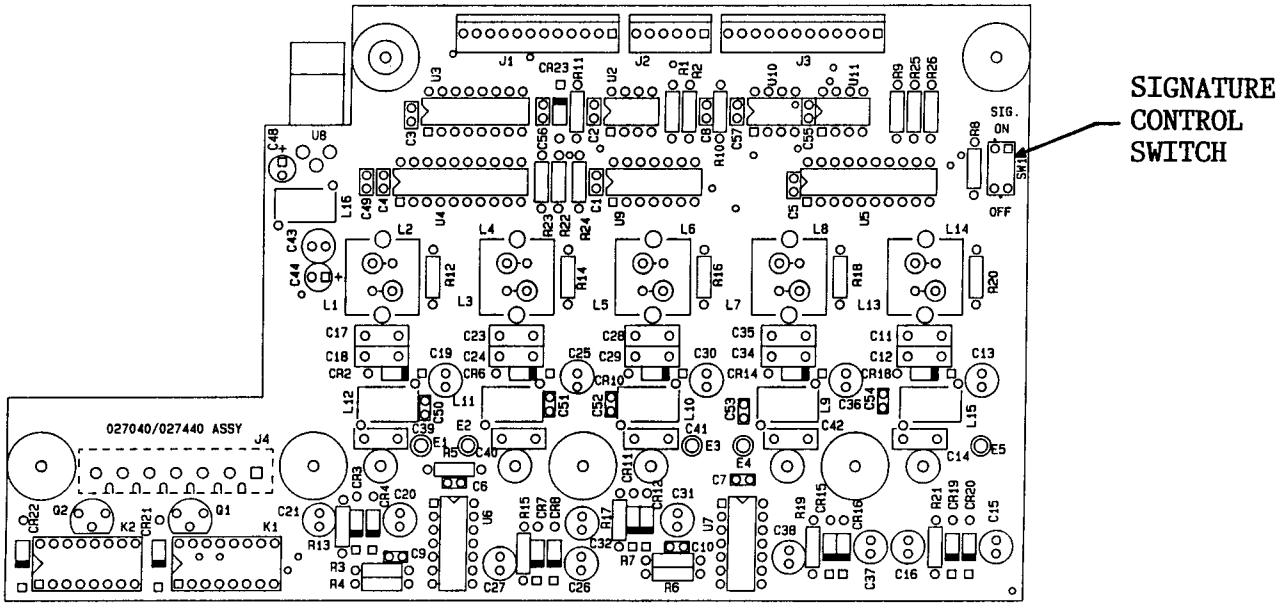


FIGURE 2-6 SIGNATURE CONTROL SWITCH

2.8 SIMULCAST TRANSMITTER OFFSETS

In simulcast radio systems, it is desirable to cover large geographic areas with multiple base station transmitters. Simulcasting requires precise control of transmitter frequencies to reduce interference between adjacent transmitters on the same channel.

Ineffective transmitter frequency control can reduce system coverage and cause "dead spots," "false pages," and message distortion. These adverse effects are reduced or eliminated by providing a carrier frequency offset between adjacent transmitters. The offset values are selected to minimize co-channel interference. To assure maximum performance of the system, the effects of transmitter oscillator "aging" must be neutralized by periodically checking and adjusting the transmitter oscillators to maintain the desired frequency offsets.

The SPECTRACOM MODEL 8165 SIMULCAST TRANSMITTER OFFSETS provides an accurate, controlled frequency reference which is "frequency locked" to the National Institute of Standards and Technology. This reference can be used by synthesized transmitters to provide "ageless" frequency control, including offsets, to within one part per billion. Optional frequency offsets are discussed in the Option Section of this manual. Other frequency offsets can be provided on a special order basis from the factory.

2.8.1 Frequency Offsets

A frequency offset is entered into the Model 8165 by dip switches A6U1-1 and A6U18-2,3,4,5. Table 2-2, FREQUENCY OFFSETS, lists the frequency of the 10-MHz standard as a function of switch settings.

TABLE 2-2

FREQUENCY OFFSETS

NOTE: Offset is positive when A6U1-1 is on, and offset is negative when A6U1-1 is off.

Offset Step	Switch A6U18 -2 -3 -4 -5 C4,C3,C2,C1	Frequency (in hertz) Positive Offset A6U1-1 = ON	Negative Offset A6U1-1 = OFF	Relative Frequency Δf_S
0	0000	10,000,000.000	10,000,000.000	0.0
1	0001	10,000,000.066	9,999,999.934	6.6×10^{-9}
2	0010	10,000,000.132	9,999,999.868	13.2×10^{-9}
3	0011	10,000,000.199	9,999,999.801	19.2×10^{-9}
4	0100	10,000,000.265	9,999,999.735	26.5×10^{-9}
5	0101	10,000,000.331	9,999,999.669	33.1×10^{-9}
6	0110	10,000,000.397	9,999,999.603	39.7×10^{-9}
7	0111	10,000,000.464	9,999,999.536	46.4×10^{-9}
8	1000	10,000,000.530	9,999,999.470	53.0×10^{-9}
9	1001	10,000,000.596	9,999,999.404	59.6×10^{-9}
10	1010	10,000,000.662	9,999,999.338	66.2×10^{-9}
11	1011	10,000,000.728	9,999,999.272	72.8×10^{-9}
12	1100	10,000,000.795	9,999,999.205	79.5×10^{-9}
13	1101	10,000,000.861	9,999,999.139	86.1×10^{-9}
14	1110	10,000,000.927	9,999,999.073	92.7×10^{-9}
15	1111	10,000,000.993	9,999,999.007	99.3×10^{-9}

The frequency correction switch, A6U1-7, must be on to allow the unit to frequency lock. An offset may be entered without removing power. Once an offset is entered a Frequency alarm occurs causing a Major Alarm. A Major Alarm removes the rear panel outputs if the signature control feature is enabled. The outputs return when the unit synchronizes to within 1×10^{-8} of the expected frequency. Once this occurs the FREQ and OUTPUT lamps are cleared by depressing the RESET button.

2.8.2 *Frequency Offset at the Carrier Frequency*

The frequency offset at the carrier frequency is determined by the formula

$$\Delta f_c = F_c \times \Delta f_s$$

where:

Δf_c = carrier offset

F_c = carrier frequency

Δf_s = offset of 10-MHz standard (from Table 2-2)

Table 2-3, OFFSET AT VHF AND UHF BANDS, lists the frequency offset in Hertz as a function of switch setting for the VHF and UHF bands.

TABLE 2-3

OFFSET AT VHF AND UHF BANDS (IN HERTZ)

NOTE: Offset is positive when A6U1-1 is on, and offset is negative when A6U1-1 is off.

Offset Step	Switch A6U18 -2 -3 -4 -5 C4,C3,C2,C1	Offset (in hertz) VHF 132 MHz	VHF 170 MHz	UHF 440 MHz	UHF 480 MHz
0	0000	0	0	0	0
1	0001	0.87	1.12	2.90	3.17
2	0010	1.74	2.24	5.80	6.34
3	0011	2.63	3.38	8.76	9.55
4	0100	3.50	4.50	11.66	12.72
5	0101	4.37	5.63	14.57	15.89
6	0110	5.24	6.75	17.47	19.06
7	0111	6.12	7.89	20.42	22.27
8	1000	7.00	9.01	23.32	25.44
9	1001	7.87	10.13	26.22	28.61
10	1010	8.74	11.25	29.13	31.78
11	1011	9.61	12.38	32.03	34.94
12	1100	10.49	13.52	34.98	38.16
13	1101	11.37	14.64	37.88	41.33
14	1110	12.24	15.76	40.79	44.50
15	1111	13.11	16.88	43.69	47.66

2.8.3 *Performance*

The Model 8165 operates on a "frequency locking" principal. The frequency of the 10-MHz standard oscillator is measured and control voltage corrections applied to bring it to the desired frequency. The time base for the measurement is derived from the received WWVB signal. The measurement interval is 1000 seconds. The measurement resolution is one part in 10 to the 10th power (1×10^{-10}). The adjustment resolution is 2.4 parts in 10 to the 10th power (2.4×10^{-10}). The long term accuracy is typically plus or minus one part in 10 to the 9th power ($\pm 1 \times 10^{-9}$). The frequency offsets may be verified by the Offset Performance Test described in Section 6.

2.9 *PRINTOUTS AND COMMANDS*

The FTC will print out a number of different records reflecting its status and monitored results. These records include:

Time Lock Step Record
Frequency Measurement Record
Valid Frequency Measurement Record
Restart Record
D/A Set Record

Examples of each of these records shown and explained below. All numeric values in the records are in hexidecimal.

2.9.1 *Time Lock Step Record*

Time Lock Step Record Printouts are preceded by an arrow (⟶) and are not applicable to the Model 8165.

2.9.2 *Frequency Measurement Record*

****TIME=080043 FREQ=0002540BE3FB DA=0554 SHIGH=00 PHASE=002F GOOD=0333 LO/H1=0000**
****TIME=08008C FREQ=0002540BE3F6 DA=0554 SHIGH=00 PHASE=002F GOOD=00F8 LO/HI=0024**

Frequency Measurement Records are generated at the end of each frequency measurement gate period. Except for testing, the gate period is 1000 seconds. SHIGH, PHASE, GOOD and LO/HI are parameters used in the Time Lock process and are not applicable to the Model 8165. TIME, FREQ and DA are explained below:

TIME This is the time in seconds since power on.

FREQ This is the actual Frequency Count in hexidecimal for the gate period. A perfect count for 1000 seconds would read: 0002540BE400.

DA This is the current D/A value at the time of the record.

2.9.3 Valid Frequency Measurement Record

****TIME=08DFD0 FREQ=0002540BE409 DA=0552 SHIGH=00 PHASE=003F GOOD=0028 LO/HI=FFDC**
DA ADJ=0066 FREQ ADJ=0066 INDX=01 LOST LOCK=0000
AVGFRR=000000000009 LAST=0552 ADJ=0003 CURR=0552

Valid Frequency Measurement Records are generated each time three Frequency Measurement Records have been generated and when three of the last three or four records indicate frequency counts which agree within 10 counts of each other (1×10^{-9}).

DA-ADJ — This is the D/A Adjustment Count. This counter counts the number of times that the D/A has been adjusted since power up. The D/A is adjusted when Valid Frequency Measurements are made.

FREQ-ADJ — This is the Frequency Adjust Count. This counter counts the number of Valid Frequency Measurements since power up.

INDX — This is the last index used in the circular table of four frequency measurements.

LOST-LOCK — This is the Lost Lock Count. This counter counts the number of times that the WWVB receiver has lost lock since power up.

AVGERR — This is the Average Error of the three frequency counts used in the Valid Frequency Measurement relative to a perfect count.

LAST — This is the current D/A value.

ADJ — This is the D/A Adjustment Value. This is the computed magnitude of the adjustment which should be applied to the current D/A value to correct for the Average Error. If the error is positive, this value will be added to the current D/A value, else it will be subtracted.

CURR — This is the new D/A value which will be used.

2.9.4 Restart Record

RESTART AT 000016

Restart Records are generated any time an "R" is typed at the terminal. Current frequency counting is aborted and restarted. The record indicates the time at which the gate period was restarted.

2.9.5 D/A Set Record

D/A SET TO 04CO AT 000014

D/A Set Records are generated any time the D/A is manually set. To set the D/A, a "D" is typed at the terminal. The value that the D/A is set "to" is shown as well as the time "at" which it was set.

2.9.6 Log Record

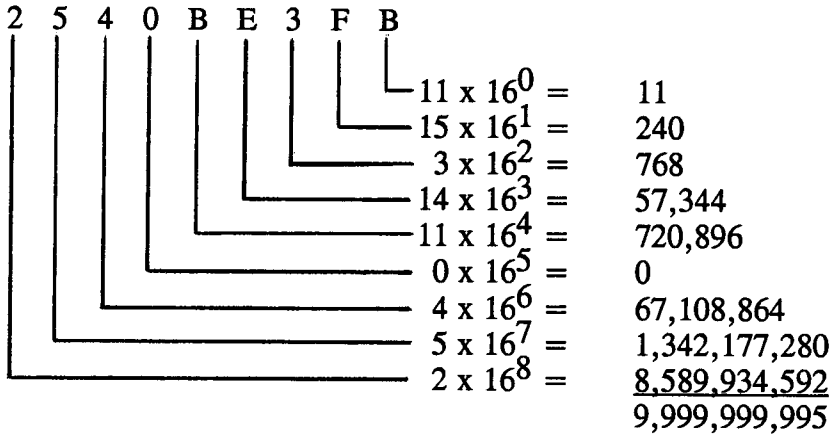
A complete log of receiver functions is printed when "L" is typed into the terminal.

2.9.7 Frequency Conversion Table

FREQ. (DECIMAL)	FREQ. COUNT (HEX) (GATE=10)	FREQ. COUNT (HEX) (GATE=1000)
10,000,002.500	000005F5E119	0002540BEDC4
10,000,000.100	000005F5E101	0002540BE464
10,000,000.050	000005F5E100	0002540BE432
10,000,000.010	000005F5E100	0002540BE40A
10,000,000.000	000005F5E100	0002540BE400
9,999,999.990	000005F5E100	0002540BE3F6
9,999,999.950	000005F5E100	0002540BE3CE
9,999,999.900	000005F5EOFF	0002540BE39C
9,999,992.50	000005F5EOB5	0002540BC6B4

2.9.8 Hexidecimal to Decimal Conversion

EXAMPLE: Find the output frequency in hertz from a printout frequency measurement of 002540BE3FB.



Divide the total number of cycles counted by the 1000 second gate period to solve for the output frequency.

$$\frac{9{,}999{,}999{,}995 \text{ cycles}}{1{,}000 \text{ seconds}} = 9{,}999{,}999.995 \text{ Hz}$$

MODEL 8165

SECTION 3

SPECIFICATIONS

SPECIFICATIONS

3.0 INTRODUCTION

This section provides specifications for the Model 8165 WWVB Disciplined Oscillator.

3.1 RECEIVER

Received Standard: 60 kHz, NIST Station WWVB. In Europe MSF.

Receiver Sensitivity: 0.4 μV rms into 50 ohms.

Minimum Field Strength: 50 μV/meter at the antenna. Installation less than 50 μV/meter requires Model 8207 Preamplifier. The Model 8207 has 40 dB of gain.

Signal-to-noise ratio: -35dB worst case to remain phase locked to the carrier.

3.2 RECEIVER OUTPUTS

Receiver outputs are located on the rear panel AUX IN/OUT connector.

3.2.1 Time Code:

BCD code recovered from WWVB broadcast. Yields day of year, minutes, hours, correction factor for conversion from atomic time (UTC) to celestial time (UT1), tens and units of years, and indicators for DST, leap year, and leap second.

Levels: Logic high, +5 VDC behind 3.3K ohms
Logic low, ground

Time Frame: 1 minute

Frame Element: 1 second

Code: Pulse Duration/Meaning
0.8 seconds/position identifier
0.5 seconds/binary 1
0.2 seconds/binary 0 or uncoded element

On Time Point: Leading edge of frame element (subtracting receiver and propagation path delays).

Receiver Delay: 17 milliseconds typical

3.2.2 Lock Status

Lock Status monitors receiver phase lock status to WWVB.

Levels: Locked-signal is +5 VDC behind 3.3K ohms
Unlocked signal is ground.

3.2.3 10 MHz Output

10 MHz signal phase locked to WWVB carrier.

Levels: Open circuit high is $\geq$3.2 VDC
low is $\leq$ 0.5 VDC.

The signal is TTL compatible into loads $\geq$ 120 ohms.

Noise Jitter: Typically 1 x 10-7 in a 1-second gate period. The amount of jitter is dependent on the S/N ratio of the received signal and antenna placement.

3.2.4 Phase Comparator Output

Used to operate a chart recorder or meter to display the relative phase of the internal standard oscillator against WWVB. Output will drive a 0-1 mA meter movement, 1500 ohm impedance maximum. 1 mA full scale represents 50 microseconds of relative time.

3.3 STANDARD FREQUENCY OUTPUTS

3.3.1 Front Panel

Single output derived from the disciplined oscillator.

Signal: 10 MHz square wave

Signal Level: Open circuit high $\geq$ 3.4 VDC
Open circuit low $\leq$ 0.5 VDC
TTL compatible in loads $\geq$ 100 ohms

3.3.2 Rear Panel

Five individually buffered outputs derived from the disciplined oscillator.

Signal: 10-MHz sinewave

Signal Level: 600 mV rms into 50 ohms

Source Impedance: 50 ohms

Harmonics: better than 30 dB down

Spurious: better than 45 dB down.

Signature Control: The rear panel outputs are removed whenever a Major Alarm occurs. The outputs are restored when the fault condition has been corrected. The signature control feature may be enabled by an internal switch located on the output board.

Option 03 Distribution Amplifier: Rear panel outputs are converted to Drive Spectracom distribution products. In this version, a 12 volt DC offset is added to the 10 MHz signal.

Distribution Loading: Up to 25 loads may be driven by the distribution amplifier. The actual number depends on the distribution device current consumption and distance from the receiver.

Cable Impedance: 50 ohms

Maximum Cable Length: Up to 25 Line Taps on one output at average of 750 ft. from base station. 1500 ft. maximum using RG-58 cable; 3000 ft. with fewer Line Taps allowed if Model 8140TA Line Amplifier is used. RG-8 cable extends distance to 3000 ft. for all 25 Taps.

3.3.3 Frequency Standard Stability

Long Term: Accuracy is typically held to within $\pm 1 \times 10^{-9}$ indefinitely when phase locked to WWVB.

Short Term: 2×10^{-10} rms over 10 successive 10-second counts.

Temperature: 0-50°C $\pm 5 \times 10^{-10}$/°C max. -30 to +50° meets FCC accuracy specifications.

Load: $\pm 1.0 \times 10^{-10}$ for any load change.

Supply Voltage: $\pm 2.5 \times 10^{-10}$ max. for $\pm 15\%$ voltage change.

Recovery: During a power failure, the oscillator control value is retained and the standby supply provides power to the oscillator. At power-on, the standard outputs return to the set frequency plus or minus any oscillator aging.

Aging Rate: 1.5 x 10^{-9}/24 hours maximum after 120 days of continuous operation. 5 x 10^{-10}/24 hours typical after 180 days of continuous operation. Unit automatically corrects for oscillator aging when phase locked to WWVB.

3.4 STANDARD FREQUENCY OFFSETS

The standard outputs may be offset a precise amount for use as a reference to simulcast and television transmitters. The offsets are dip switch programmable.

Standard Offsets: 10 MHz output is offset in 6.6 x 10^{-9} steps. Selectable 15 steps positive or negative offsets.

Option 31 10 Hz TV Channel Offsets: Provides an addition $\pm$10 Hz offset when translated to the visual carrier frequency.

Option 56 Smaller Paging Offsets: 10 MHz output is offset in 1.1 x 10^{-9} steps. Selectable 15 steps positive or negative offsets.

3.5 STANDBY SUPPLY

The standby supply provides power to the oscillator when AC power is lost preventing retrace problems when AC is returned.

Battery Pack: Allows 50 hours typical at 25°C, 36 hours minimum of standby operation. The batteries are float charged whenever AC power is present. Recharge rates 33% in 6 hours, 66% in 12 hours, 100% in 36 hours.

External: Provisions for an external battery pack are made on the rear panel AUX IN/OUT connector. The battery will be float-charged whenever line power is on. The maximum charge rate is 250 mA. Recommended battery type is sealed lead-acid, 24 VDC, 1-2 A-H or greater capacity. The OVEN DC switch must be in the EXT position.

Option 55, External DC Oven Power: Replaces internal battery pack with a DC-DC converter assembly. Accepts an input voltage range of 18.7 to 36.7 VDC, requires 6.5 watts.

3.6 INDICATORS AND ALARMS

3.6.1 ALARM LAMPS

LOCK: Receiver is phase-locked to WWVB carrier.

UNLOCK: Receiver is not locked to WWVB carrier.

FREQ: Standard oscillator is off frequency by more than 1 x 10^{-8}.

SIGNAL: Lamp is on if receiver phase lock is lost for more than 10 hours.

OUTPUT: Indicates the disappearance of standard output signal from any of the five rear-panel outputs.

CPU: Indicates microprocessor failure.

ADJUST OSC: Standard oscillator has aged so that the microprocessor must pull it to within 1 x 10^{-7} of adjustment limit range. Warns that internal oscillator requires adjustment within three months.

3.6.2 Alarm Classification

MAJOR ALARM: Asserted by a FREQ, SIGNAL, or CPU alarm.

MINOR ALARM: Asserted by an OUTPUT or ADJUST OSC. alarm.

3.6.3 Remote Alarm Outputs

RS-422 Outputs: MAJOR and MINOR alarm status is output in RS-422 levels. Signals provided on AUX IN/OUT connector.

Relay Alarm Outputs: MAJOR and MINOR alarm relay contacts are provided on the rear panel output alarm connectors. The relays are Form C, 2A, 30 VDC rated.

Alarm Reset: CPU remote alarm output must be reset manually with front panel **RESET** button. All other remote alarm outputs are self-resetting when the fault condition is cleared. All alarm lamps stay on until **RESET** button is pressed.

3.7 DATA PORT

Communicates status information to an RS-232 terminal.

Signal: RS-232C

Character Structure: 1 start bit, 7 data bits, 1 mark bit, and 1 stop bit.

Baud Rate: Dip switch programmable from 300 to 9600 baud.

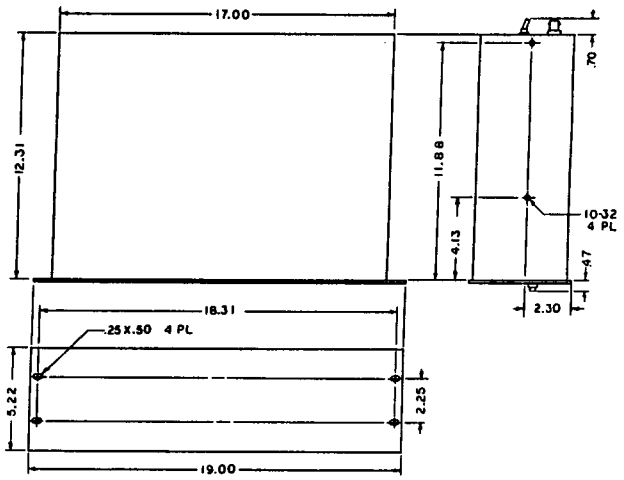
3.8 INPUT POWER

Standard: 115 VAC ± 15%, 60 Hz. Consumes 60 VA

Option 52, 12 VDC: ±13.8 VDC ± 20%, 25 watts
Option 53, 24 VDC: ±27.6 VDC ± 20%, 25 watts
Option 54, 48 VDC: ±55.2 VDC ± 20%, 25 watts

3.9 MECHANICAL

Dimensions:



Weight: 20 lbs.

Shipping Weight: 25 lbs. (11.3 Kg)

3.10 MATING CONNECTORS

Antenna, Standard Outputs: BNC male

Aux IN/Out: Molex 15 pin, male, supplied

Alarm Output: 7 position terminal block, supplied

Data: 9 pin series D, male

3.11 ENVIRONMENTAL

Operating Temperature: -30 to +50°C

Storage Temperature: -40 to +85°C

3.12 MISCELLANEOUS

Patent No: 4,525,685

Traceability: WWVB identifies itself by advancing its carrier phase by 45° at 10 minutes after every hour and returns to normal phase at 15 minutes after the hour. This station identifier can be seen on the phase comparator output. It appears as a step voltage change on a voltmeter or as a 2.1 microsecond phase shift on a chart recorder.

MODEL 8165

SECTION 4

PRINCIPLES OF OPERATION

PRINCIPLES OF OPERATION

4.0 INTRODUCTION

The Model 8165 Disciplined Oscillator consists of an RF Amplifier Assembly, a Receiver Assembly, an Oscillator and Power Supply Assembly, an Output Amplifier Assembly, and a Frequency and Time Control Assembly (FTC) as shown in the Block Diagram, Figure 4-1 and Mainframe Schematic Diagram, Figure 4-2.

The 60-kHz output of the RF Amplifier Assembly is fed to the Receiver Assembly where the carrier is detected and translated to a phase locked 10-MHz. The AGC voltage is generated in the Receiver Assembly for use in controlling the gain of the RF Amplifier during phase lock conditions.

The output of the 10-MHz frequency standard, located on the Oscillator and Power Supply Assembly, is fed to the Output Amplifier Assembly for distribution and is also divided down to 100-kHz for phase comparison with the WWVB-derived signal.

The NIST 10-MHz signal is fed to the FTC Assembly and used as a time base for measuring the STD 10-MHz signal.

4.1 RF AMPLIFIER A1 (P/N 001100)

The RF Amplifier Assembly filters and amplifies the signal. Figure 4-3 is the schematic diagram and Figure 4-4 is the component location diagram.

The signal from the antenna is applied to T1 which matches the 50-ohm input impedance. The secondary of T1 and C2 form a 60-kHz tuned circuit with a 200-Hz bandwidth. The output of Q1 is applied to a bandpass filter, made up of Q2, Y1, C7, C8, C9, and C10. The filter bandwidth is 30 Hz, with C8 trimming the bandpass center frequency at 60 kHz. C9 and C10 couple to the output of Y1 a signal that is 180° out of phase and tuned to null 100 kHz. This tuning provides a sharp bandpass response at 60 kHz with very steep high frequency rejection.

The output of the crystal filter is fed to U1. The output of U1 is tuned by L3, C14, C15, and C23. Amplifier U1 provides AGC for the receiver. Trimmer R19 provides AGC level adjustment to U1 at the gain control input U1 Pin 5. The output of U1 is coupled to U2 by C16. The output of U2 goes to emitter follower Q3 providing the output signal to the A2 Receiver Assembly through P2-3.

The +12 VDC supply voltage from the A2 Assembly enters the board at P2-1 through R18, L2, and L1, to power the amplifier stages. The 12 volts also goes to S1, R2, and through T1 to provide power to the antenna preamplifier. If a MODEL 8207 LINE PREAMPLIFIER is used, S1 should be set to P.

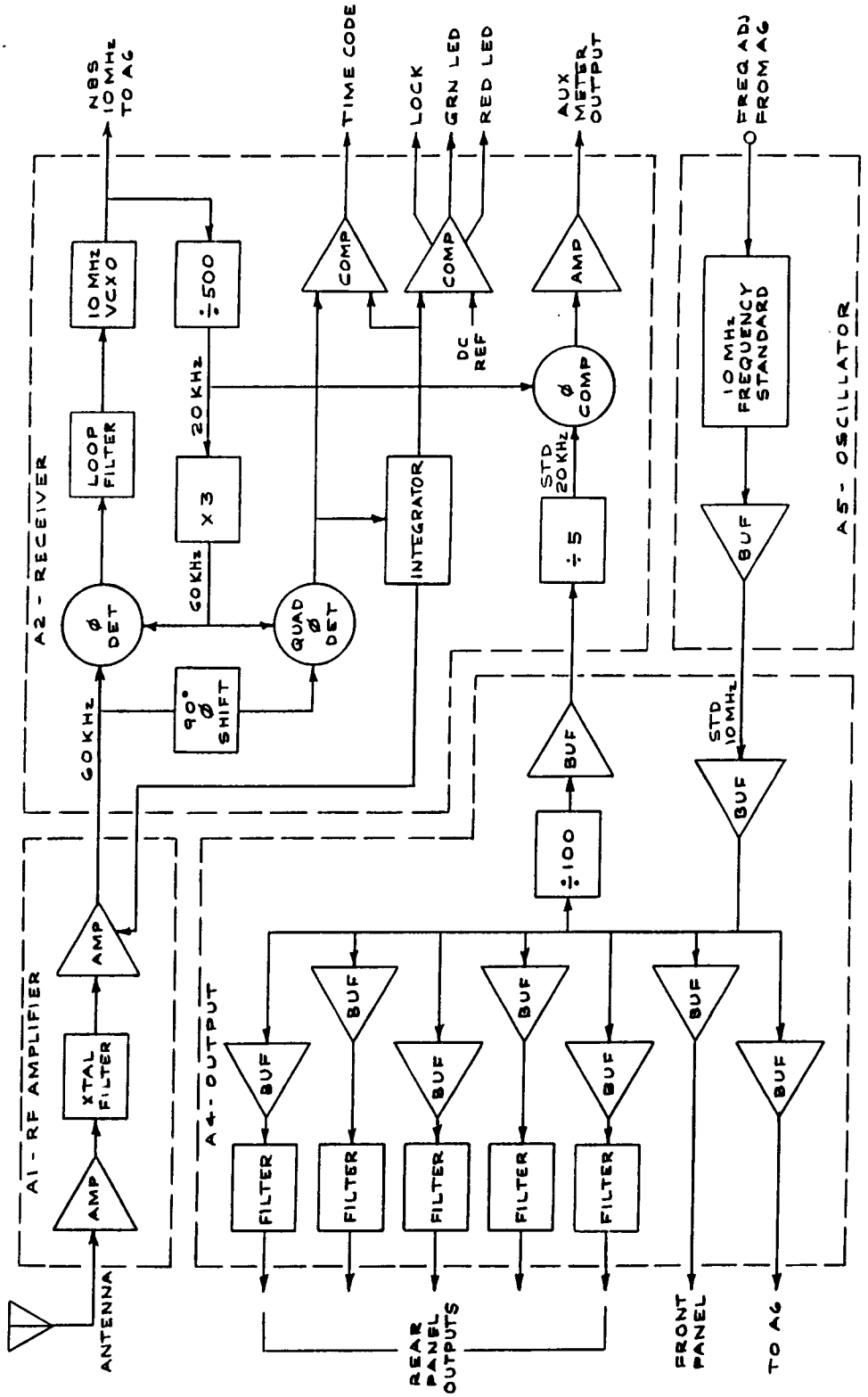


FIGURE 4-1 MODEL 8165 RECEIVER BLOCK DIAGRAM
SHEET 1 OF 2

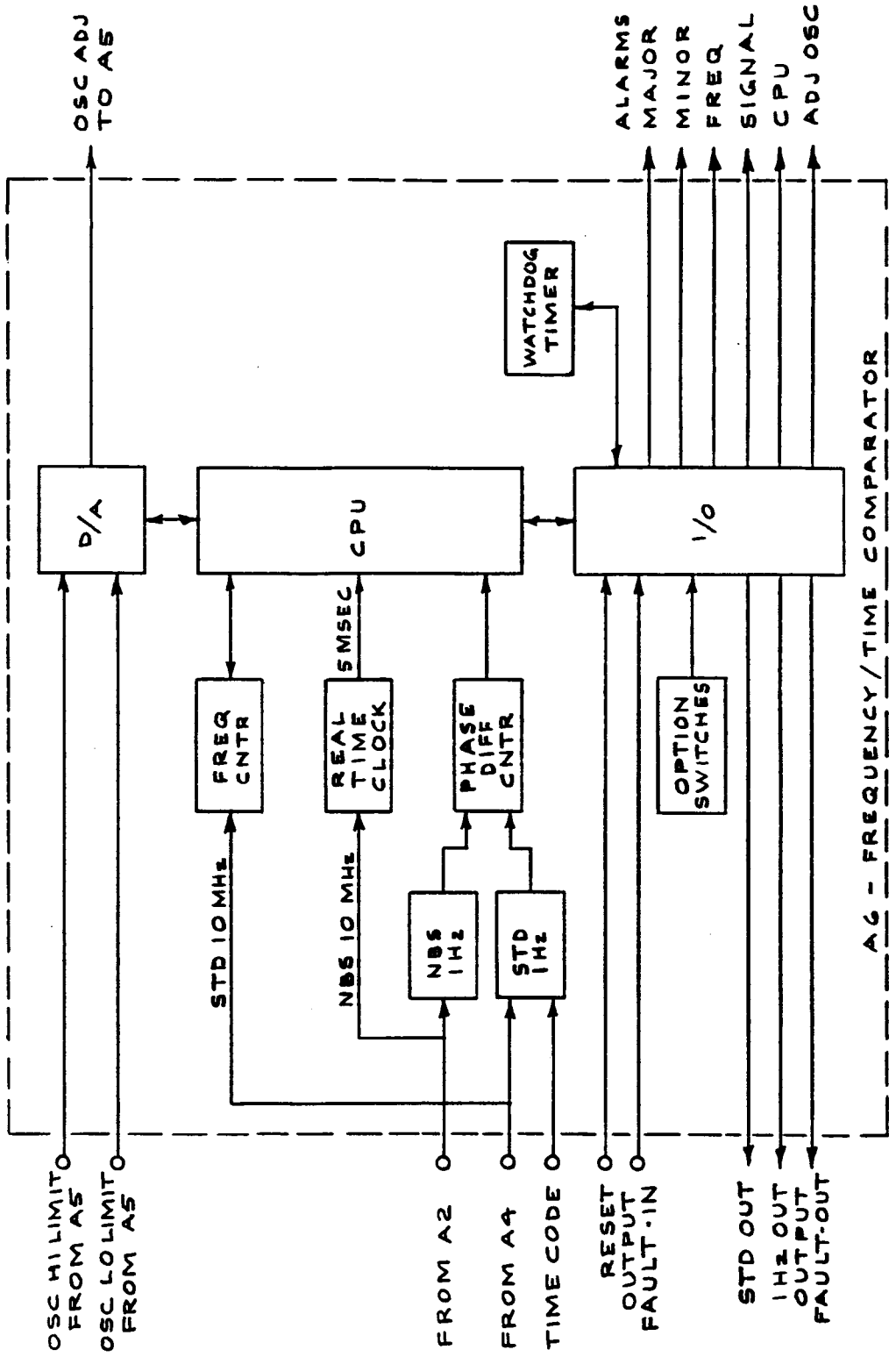


FIGURE 4-1 MODEL 8165 RECEIVER BLOCK DIAGRAM SHEET 2 OF 2

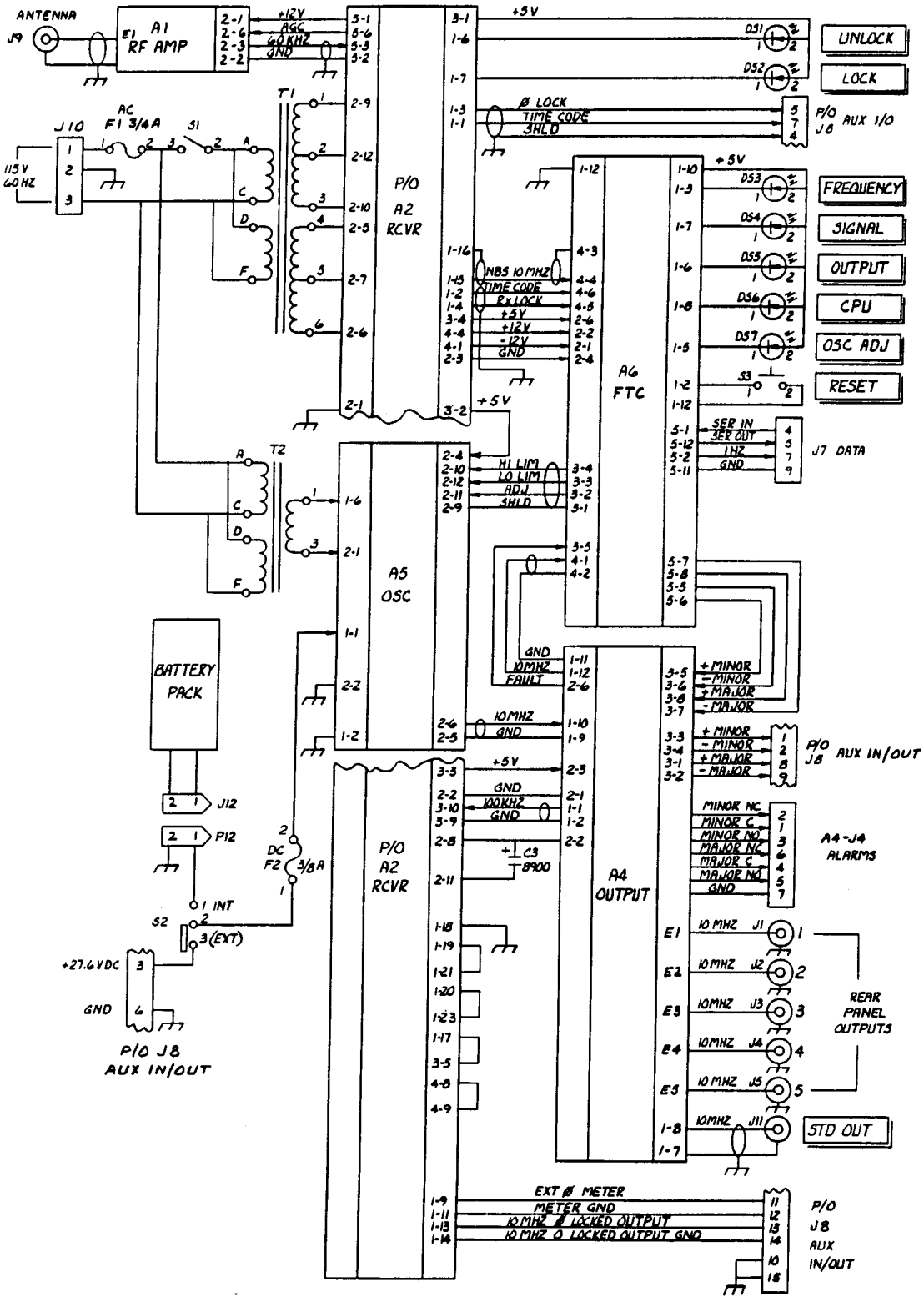


FIGURE 4-2 MODEL 8165 MAINFRAME SCHEMATIC DIAGRAM

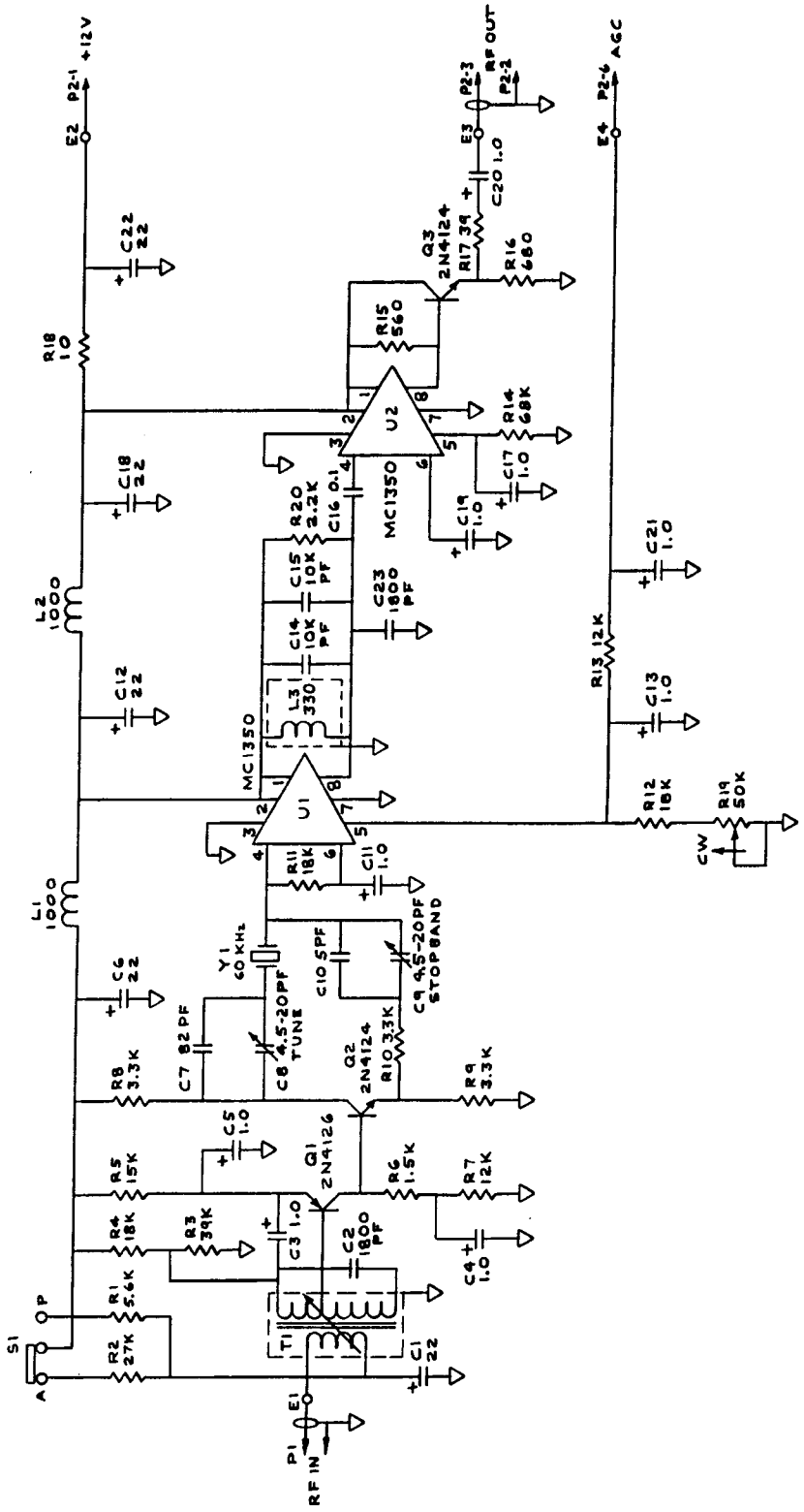


FIGURE 4-3 RF AMPLIFIER A1 SCHEMATIC DIAGRAM

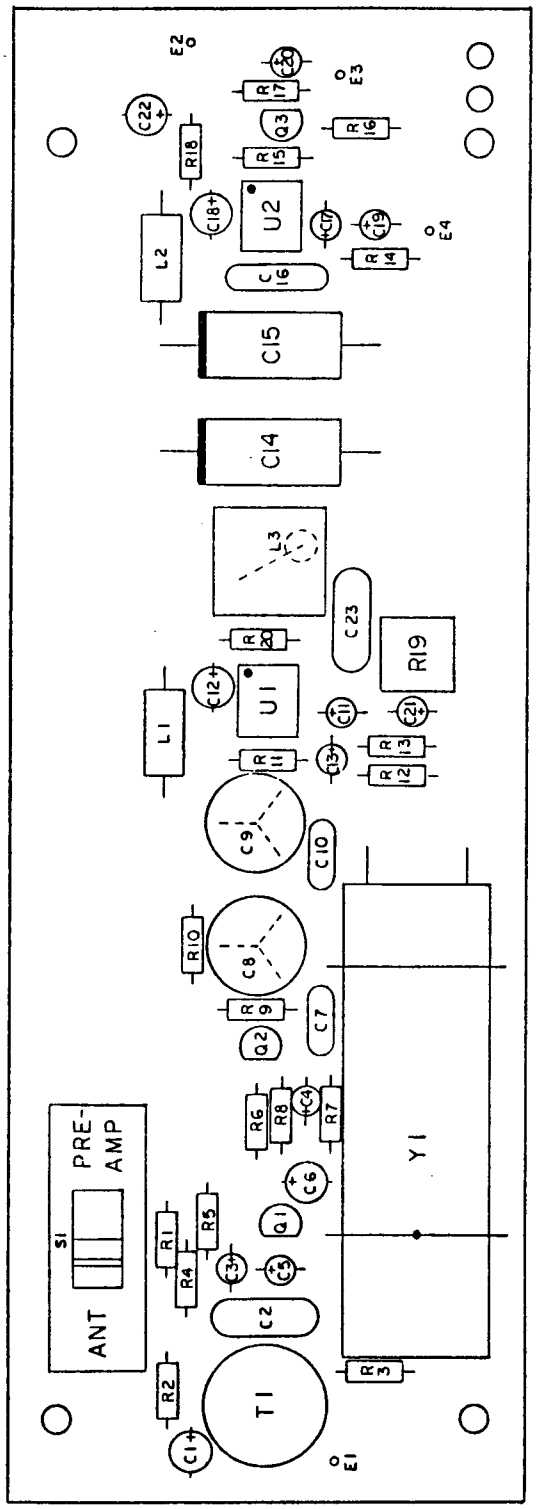


FIGURE 4-4 RF AMPLIFIER A1 COMPONENT LOCATION DIAGRAM

4.2 RECEIVER ASSEMBLY A2 (P/N 001200)

The Receiver Assembly A2 functions are:

1. Provides synchronous detection of the carrier frequency and translates it to 10-MHz.
2. Provides AGC voltage.
3. Time code detection.
4. Phase lock/unlock indication.
5. Compares the standard oscillator with the phase locked oscillator output to determine frequency error.
6. The +12 VDC, -12 VDC, and +5 VDC power supplies are located on this assembly.

Figure 4-5 is the schematic diagram. Figure 4-6 is the component location diagram.

The signal from the RF Amplifier Assembly is fed into connector J5-3. It goes to the phase locked loop, U1 and U2A, which provides synchronous detection of the carrier frequency and translates it to 10-MHz. The signal also goes through U3 and U2B to provide AGC voltage, time code detection, and phase lock/unlock indication.

4.2.1 Phase Locked Loop

The reference input to the phase detector U1-1 comes from the A1 Assembly. The comparison frequency input to phase detector U1- 8 is derived from the phase locked oscillator. The output from U1 is a DC voltage which is a function of the phase difference of these 60 kHz signals. The output is amplified by U2A, the loop filter/amplifier. This amplified DC voltage is further amplified by Q2 and Q3 where it becomes the VCO control voltage which tunes the oscillator (Q4 and Y1) into phase lock with the incoming carrier frequency from WWVB. This oscillator tuning is performed by the DC voltage which appears on the cathode of the varicap CR2. The oscillator output frequency is held exactly at 10 MHz by the DC voltage applied to the VCO control line. The collector output from Q4 is buffered by gate U5A and divided by U8, U9, U10, and U16.

The 20 kHz output is injected to tripler stage Q9 where the output, 60 kHz, is filtered and fed back into the comparison input of phase detector U1-8. The phase locked loop translates the incoming 60 kHz carrier frequency from WWVB to 10 MHz at the crystal oscillator output, and divides it down to 60 kHz for comparison in the phase detector.

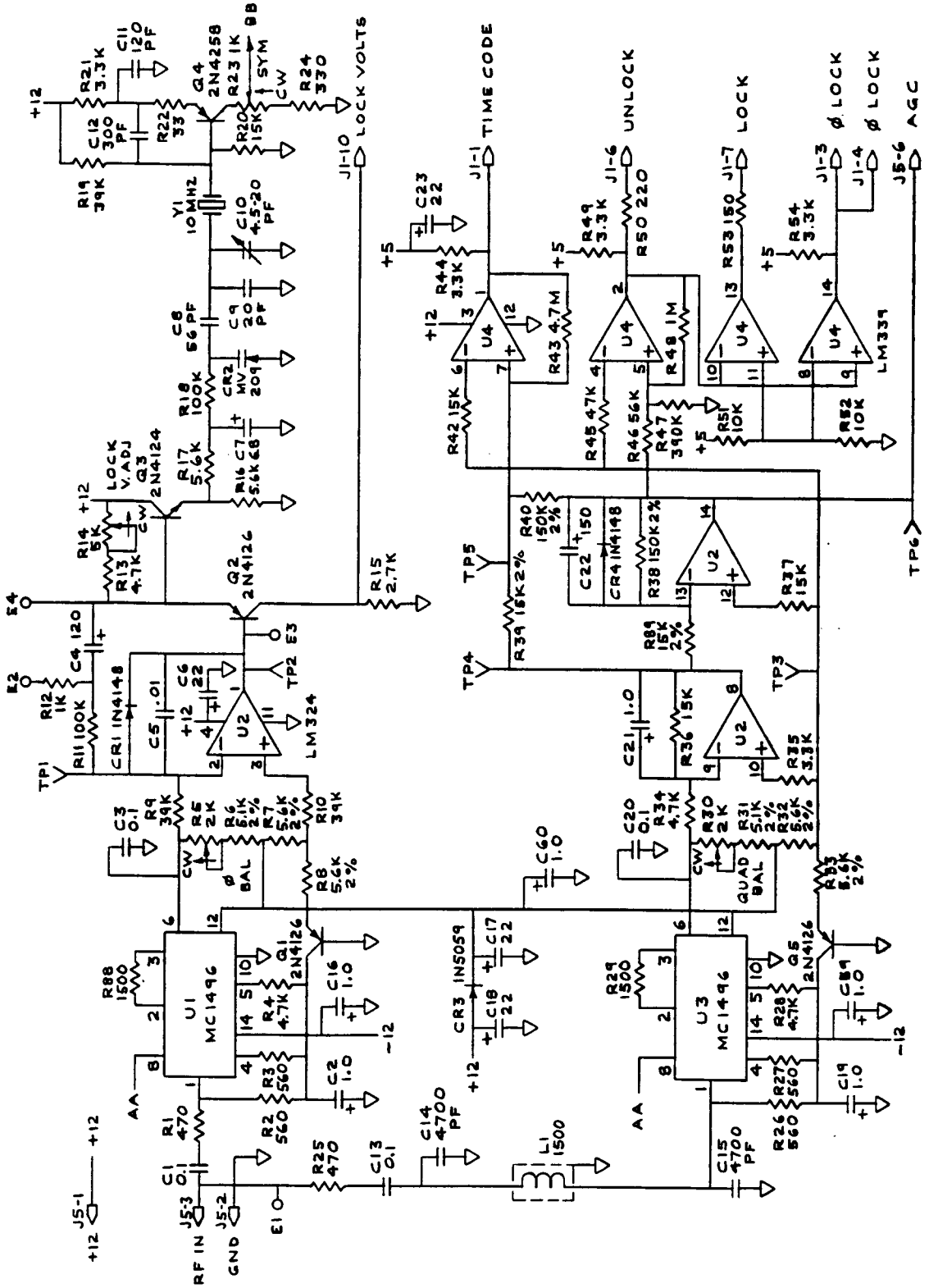


FIGURE 4-5 RECEIVER ASSEMBLY A2 SCHEMATIC DIAGRAM SHEET 1 OF 3

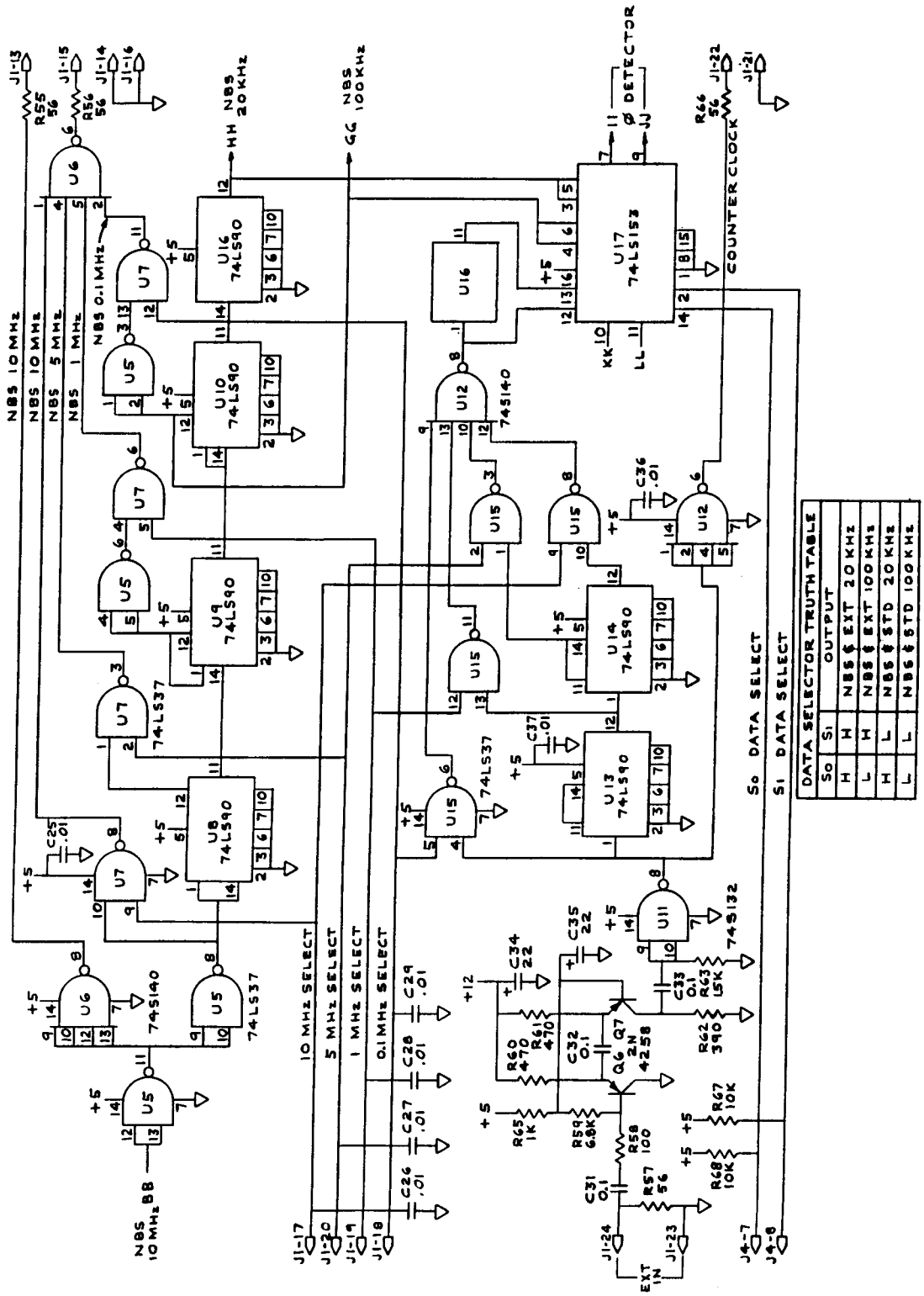


FIGURE 4-5 RECEIVER ASSEMBLY A2 SCHEMATIC DIAGRAM SHEET 2 OF 3

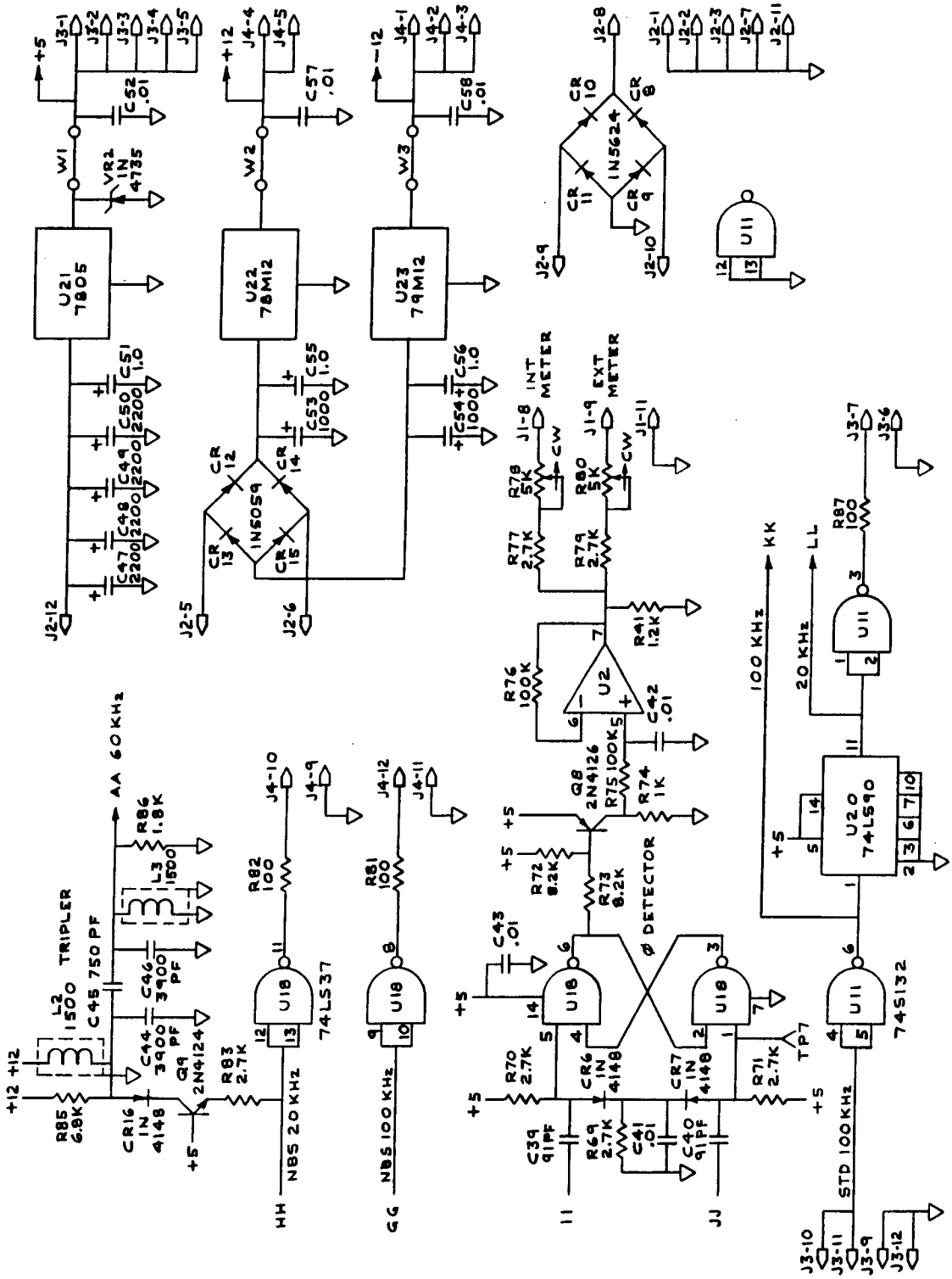


FIGURE 4-5 RECEIVER ASSEMBLY A2 SCHEMATIC DIAGRAM SHEET 3 OF 3

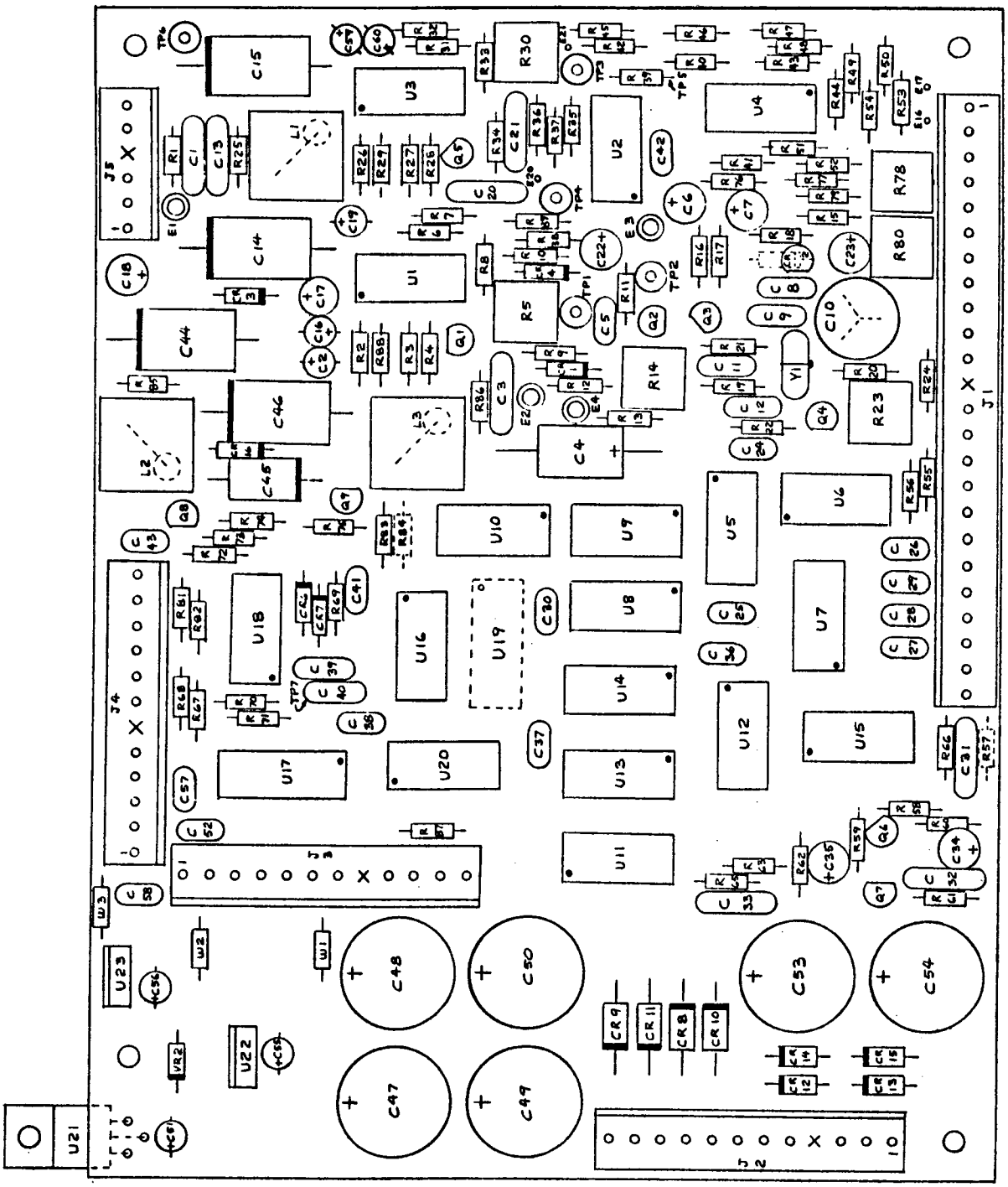


FIGURE 4-6 RECEIVER ASSEMBLY A2 COMPONENT LOCATION DIAGRAM

4.2.2 AGC Loop

The input from the RF Amplifier A1 goes to U3-1 phase detector after being shifted in phase 90° by C14, C15, and L1. U3-6 quadrature phase detector output goes high only when the inputs at U3-1 and U3-8 are in quadrature at 60 kHz. The output level from this phase detector is proportional to the level of the incoming carrier, and provides the basis for time code amplitude detection, and AGC voltage generation.

The phase detector output is amplified by U2B, whose time constant is approximately 15 milliseconds. The output of U2B is split in two directions: first, through R39 to voltage comparator U4A where small amplitude variations in signal are detected and provide the time code output. Second, through R89 to amplifier U2C that has an integrating time constant of approximately 25 seconds. The slowly varying output of U2C is used as the AGC voltage. This AGC voltage is fed back to the RF Amplifier A1 to control the gain of the input stage.

Because the AGC voltage is derived from the output of a quadrature detector, it is present only after phase lock is achieved, and becomes the basis for synchronous AGC. The gain of the amplifier in the front end of the receiver is running wide open until phase lock occurs. After phase lock is achieved the input amplifier gain is reduced to a level sufficient to provide a reference for the phase locked loop and other stages in the Receiver Assembly A2. No stages are allowed to saturate or be overdriven in strong signal conditions.

TP3 is located at the reference voltage against which AGC amplifier U2C operates. The voltage measured from TP3 to TP6 is proportional to the input signal level and can be used as an indication of signal strength. If the antenna is adjusted and aimed to maximize this AGC voltage, optimum receiver operation is obtained.

The AGC voltage is used by the voltage comparators U4B, U4C, and U4D to indicate phase lock. When the AGC voltage measured from TP3 to TP6 rises to approximately 1.0 VDC, the output of comparator U4B goes high turning off the red UNLOCK front panel indicator. When lock is acquired, the output of U4D goes high and lights the LOCK indicator via J1-3.

4.2.3 Phase Detector Balance Adjustment

The phase detector output U1 of the phase locked loop control is balanced by adjustment of trimmer R5. The output of the quadrature phase detector U3 is balanced by adjusting trimmer R30.

4.2.4 Phase Comparator

The phase comparator data selector U17 is permanently wired to send 20 kHz NIST and Standard Oscillator signals to the phase comparator. The operation of data selector U17 is shown in the truth table on Sheet 2 of the A2 Receiver Assembly Schematic. The two outputs from U17 are chosen by selecting the appropriate combination of highs and lows on inputs 2 and 14. Referring to the truth table for data selector U17, we can see that if Pin 2 is low and Pin 14 is high, then output Pins 7 and 9 will provide NIST 20 kHz and Standard Oscillator 20 kHz to the phase detector inputs. Under this

condition the phase detector output will cause an external meter to read 50 microseconds full scale (the reciprocal of 20 kHz is 50 microseconds, or one full cycle of a 20 kHz signal).

U18A and U18B are connected as a flip-flop phase detector whose output pulse width is proportional to the relative phase relationship between the two input signal pulses. Buffering of this output pulse is provided by Q8, and integration by R75 and C42. Buffer amplifier U2D then drives the rear panel auxiliary output for an external meter or chart recorder. Full scale adjustments are made by adjusting the current to ground through a milliammeter at the output to exactly 1.0 mA and with TP7 grounded, causing the phase detector to indicate full scale. Trimmer resistor R80 adjusts full scale setting of the rear panel output.

4.2.5 Power Supplies

Three terminal regulators U21, U22, and U23 provide output voltages of +5.0 volts, +12.0 volts, and -12.0 volts. Because U21 which provides the +5.0 volts is the most heavily loaded of the voltage regulators, it is heat sunk to the chassis at the rear left corner of the circuit board. Regulators U22 and U23 are more lightly loaded and do not require heat sinking.

4.3 OUTPUT/DISTRIBUTION AMPLIFIER A4 (P/N 27040/027040A)

The internal frequency standard oscillator output is fed to the 10-MHz standard input of the A4 Assembly at J1-10 where it is buffered by U2. See Figure 4-7, A4 Output/Distribution Amplifier Schematic Diagram, and Figure 4-8, A4 Component Location Diagram. The 10-MHz signal is then passed through U9 to the line drivers U4 and U5. The outputs of the line drivers are filtered to a sinewave. Diodes 2, 6, 10, 14, and 18 allow current sinking by the output drivers to interface with unterminated TTL loads if desired. If the outputs are terminated with 50 ohms the sinewave output level drops to approximately 0.5V rms.

The presence of output signals at the rear panel jacks are sensed by level detectors at each output. The detector outputs are combined by comparators U6 and U7 to feed the output fault alarm to the FTC board. Any missing output will light the **OUTPUT** lamp.

The A4 board also sends the 10-MHz standard oscillator signal to the CPU assembly and 100 kHz to the receiver board assembly.

The MAJOR and MINOR ALARM signals from the CPU board are passed through the output board to operate the alarm relays. The MAJOR ALARM relay is de-energized for an alarm and the contacts are brought out on A4-J4 on the rear panel. Pin 4 is connected to Pin 6 for a MAJOR ALARM.

The MINOR ALARM relay is energized for MINOR ALARM and A4-J4 Pin 1 is connected to Pin 3.

The signature switch, SW1 on the output board defeats the alarm function of removing rear panel outputs for a MAJOR ALARM when in the OFF position.

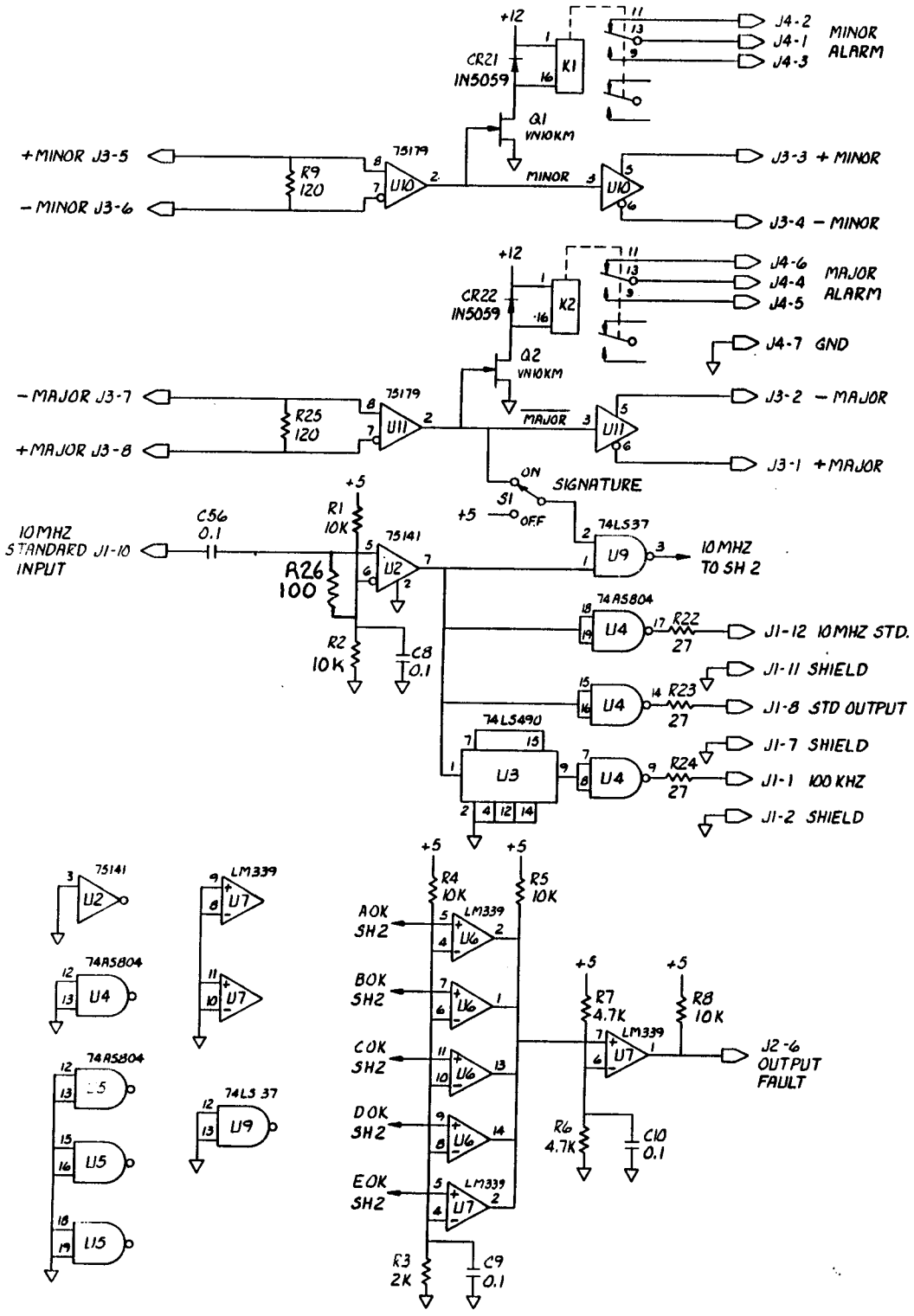


FIGURE 4-7 OUTPUT/DISTRIBUTION AMPLIFIER A4 SCHEMATIC DIAGRAM SHEET 1 OF 2

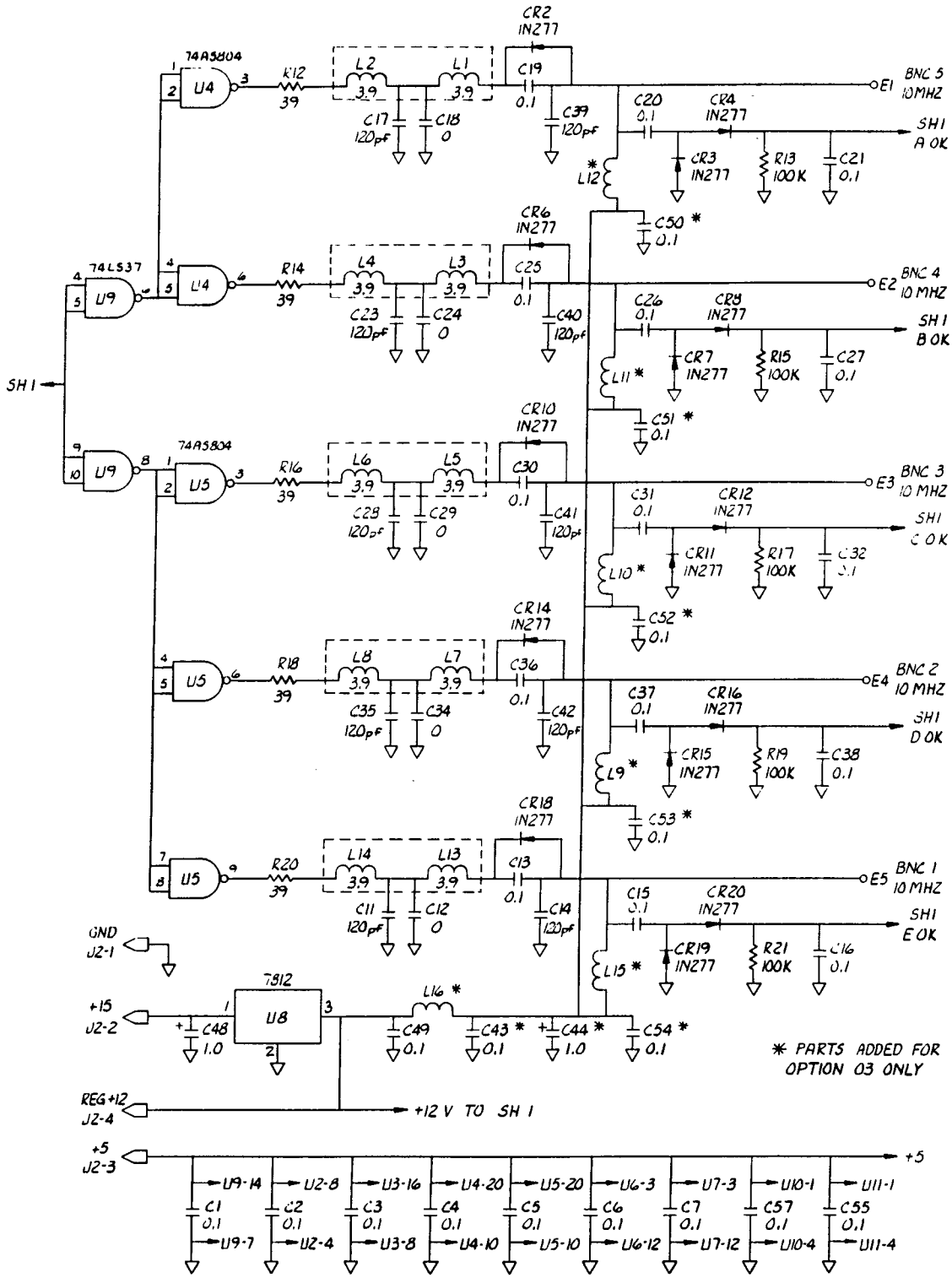


FIGURE 4-7 OUTPUT/DISTRIBUTION AMPLIFIER A4 SCHEMATIC DIAGRAM SHEET 2 OF 2

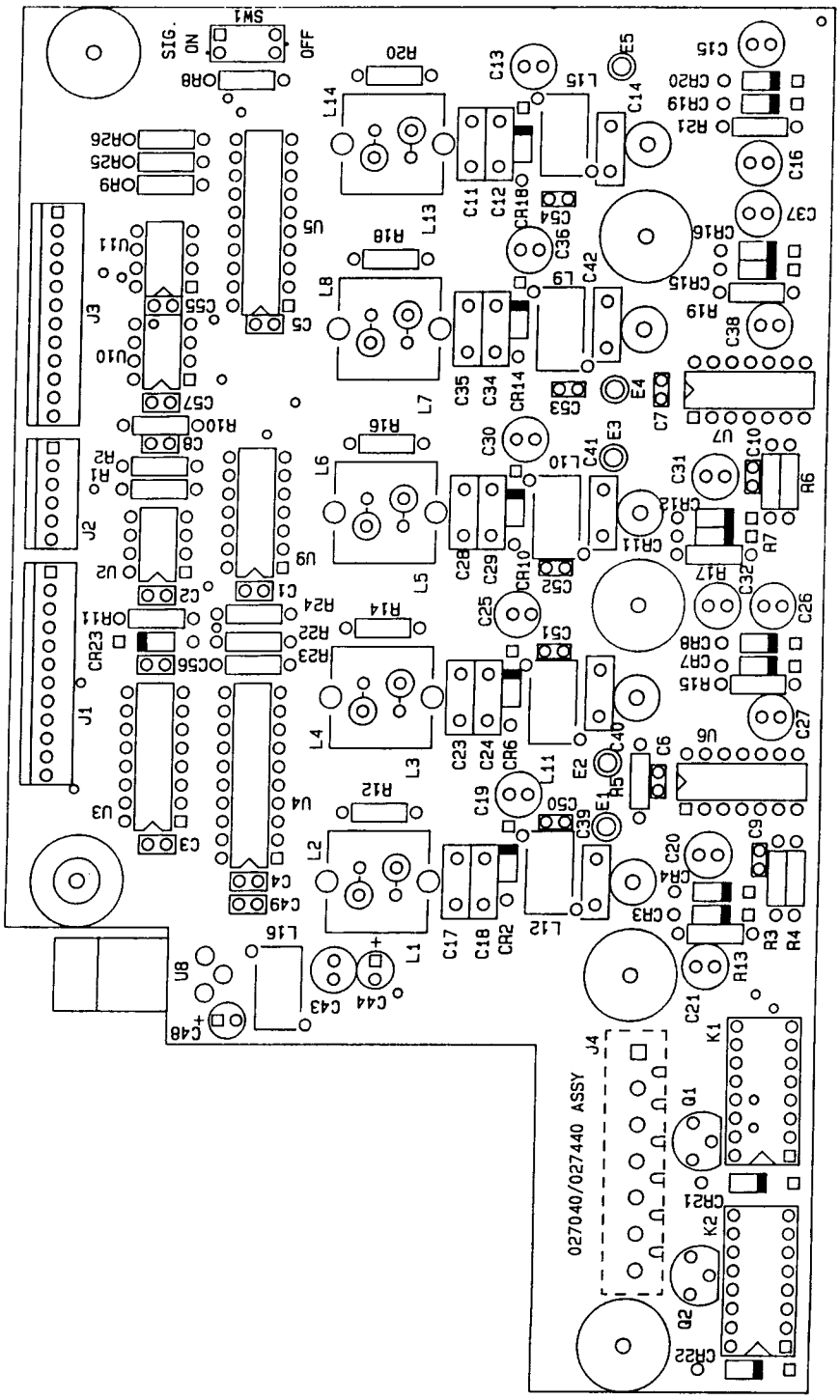


FIGURE 4-8 OUTPUT/DISTRIBUTION AMPLIFIER A4 COMPONENT LOCATION DIAGRAM

4.4 OSCILLATOR AND POWER SUPPLY ASSEMBLY A5 (P/N 002500)

Oscillator U1 is a high-stability, oven-controlled quartz crystal oscillator. The board consists of control circuitry and an oscillator power supply. The output frequency from the board is 10.0 MHz. Refer to Figure 4-9 for the schematic and Figure 4-10 for the component location diagram.

4.4.1 Oscillator Control Circuitry

The +5 volts DC is fed into the oscillator at Pin 1 where it drives the output stages and the output buffer stage Q1. The +21 volts DC is fed into Pin 5 of the oscillator where it powers the oven and the oscillator. This voltage is double- regulated and filtered extremely well before it reaches the oscillator.

4.4.2 Voltage Regulators

A diode bridge consisting of CR1 through CR4 feeds the primary regulator Q5, Q6, Q7, Q8, and Q10. Current is limited by Q5 as sensed at R14 and voltage is limited by Q8 as sensed by the voltage divider in its base circuit and VR1. Q10 provides output limiting for both voltage and current and holds the output voltage at the cathode of CR7 at exactly 27.6 volts.

If battery power supply is provided, the battery is connected at the cathode of CR7 via the battery fuse. A 24-volt lead-acid battery will be trickle-charged at 27.6 volts continuously when connected at this point. Maximum battery charging current under low charge conditions is approximately 200 milliamps, and final trickle-charge level is about 2.0 milliamps under full charge conditions.

If the primary power is disconnected from the unit, diode CR7 becomes back-biased by the battery voltage, effectively removing the primary voltage regulator from the circuit, and power is furnished to the secondary regulator U2 by the battery.

Regulators U2 and series pass transistor Q9 drop the battery voltage and regulate it at 21.0 volts DC to power the oscillator and oven.

4.4.3 Voltage Adjustments

Primary output regulator voltage of 27.6 volts at +25°C is adjusted at trimmer resistor R18. This voltage should be adjusted by -50 millivolts per degree C if the temperature varies from +25°C. This provides optimum battery charging performance. Secondary regulator output voltage is adjusted to exactly 21.0 volts DC by trimmer resistor R25.

4.4.4 Oscillator Adjustments

The oscillator coarse frequency adjustment and trimmer resistor R4 are used for centering the oscillator frequency (only after 24 hours of warm-up) and for calibrating the control voltage.

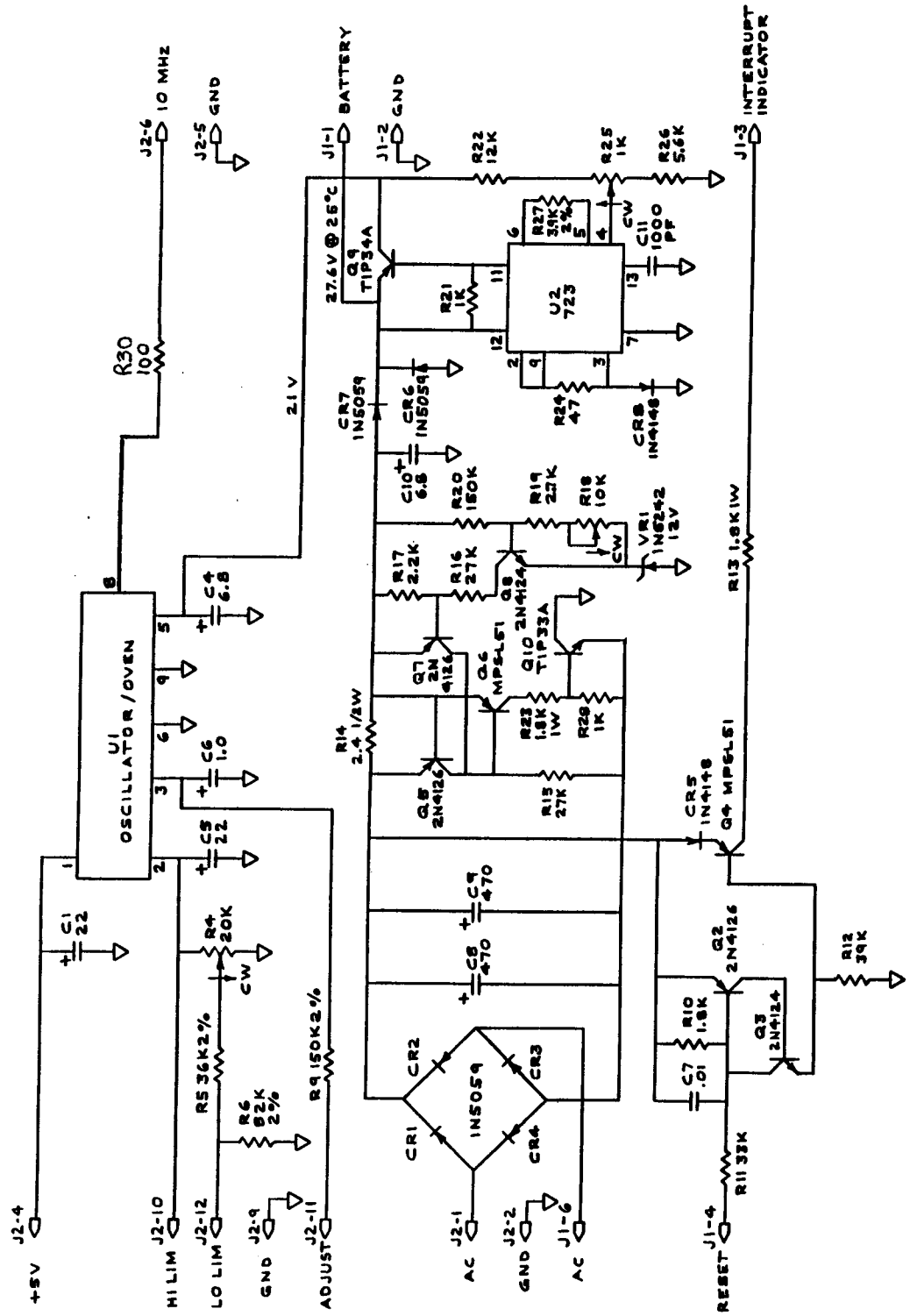


FIGURE 4-9 OSCILLATOR AND POWER SUPPLY A5 SCHEMATIC DIAGRAM

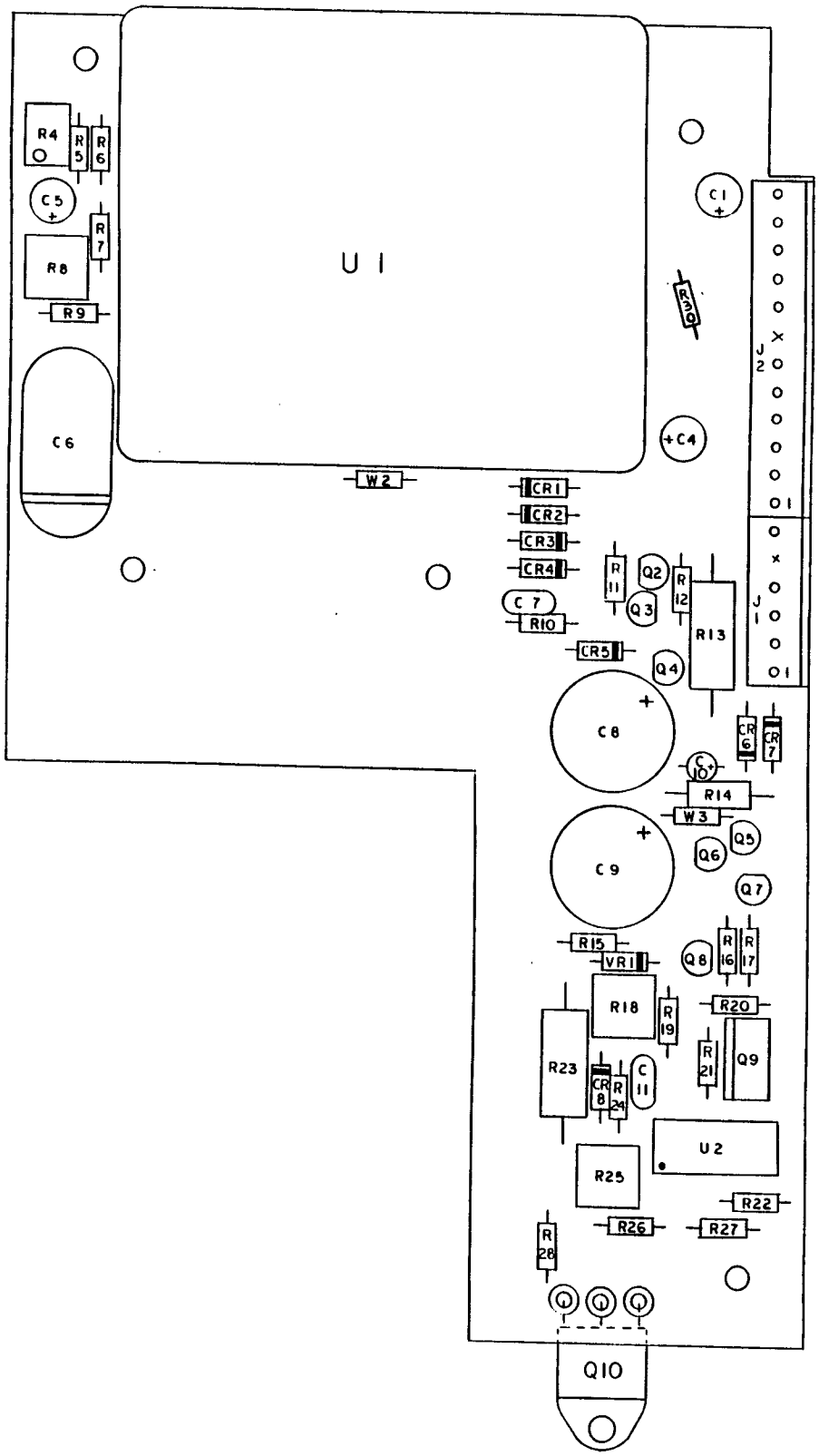


FIGURE 4-10 OSCILLATOR AND POWER SUPPLY A5 COMPONENT LOCATION DIAGRAM

4.5. FREQUENCY AND TIME COMPARATOR A6 P/N 018100

The Frequency-Time Comparator (FTC) consists of a number of functional elements including:

1. Central Processing Unit
2. Realtime Clock
3. Frequency Counter
4. NIST 1-Hz Clock
5. STD 1-Hz Clock
6. Phase Difference Counter
7. D/A Converter
8. Miscellaneous I/O

The Central Processor provides for the overall control and logical operation of the FTC. The Central Processor is an 8031 and associated peripheral circuits including external ROM and RAM.

The Realtime Clock (RTC) provides a timing reference for software controlled activities such as the frequency counter gate and time code (TCODE) decoding. The RTC provides interrupts to the processor at 5 millisecond intervals. The RTC is derived by dividing down the NIST-10 MHz from the WWVB phase-locked receiver.

The Frequency Counter provides for the measurement of the frequency of the STD 10-MHz oscillator. The gate for the counter is derived from the NIST 10-MHz which is phase locked to the WWVB carrier. Frequency counting provides for the accurate control of the frequency standard.

The NIST 1-Hz is derived by dividing down the NIST 10-Mhz and is used in decoding the time code (TCODE) received by the WWVB receiver as well as providing a reference for determining the cumulative time error.

The STD 1-Hz is derived by dividing down the STD 10-MHz. This division process provides for the tracking of cumulative frequency error in the standard.

The Phase Difference Counter provides for the reading of the phase difference between the NIST 1-Hz and the STD 1-Hz. The phase difference represents the actual cumulative frequency error, where the NIST 1-Hz is used as the reference and the STD 1-Hz is used as the accumulator.

The frequency of the standard 10 MHz is adjusted by a control voltage which is provided by the D/A converter. The Central Processor, through the frequency counter, will continuously make measurements of the standard 10 MHz. As frequency adjustments are required, the central processor will make them by changing the VCO control voltage fed to the oscillator from the D/A converter.

As a part of operating software, the central processor is required to periodically generate an output pulse to the Watchdog Timer. The Watchdog Timer will generate an alarm if the periodic pulses are not received. This provides a basic "sanity" check and alarm for the central processor.

Figure 4-11 is the schematic for the FTC board and Figure 4-12 is the assembly drawing. The following subsections discuss its functions.

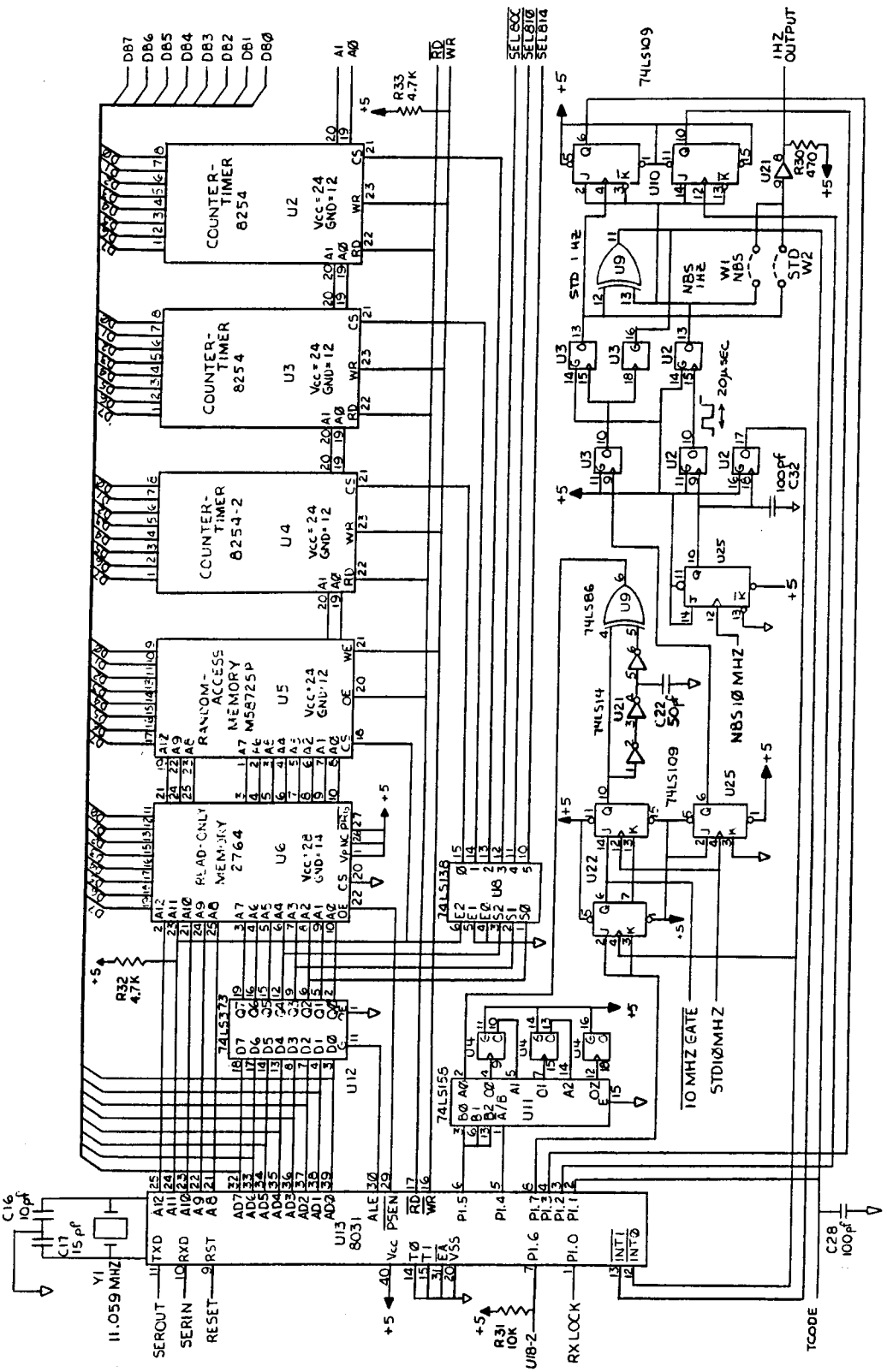


FIGURE 4-11 FTC A6 SCHEMATIC DIAGRAM
SHEET 1 OF 2

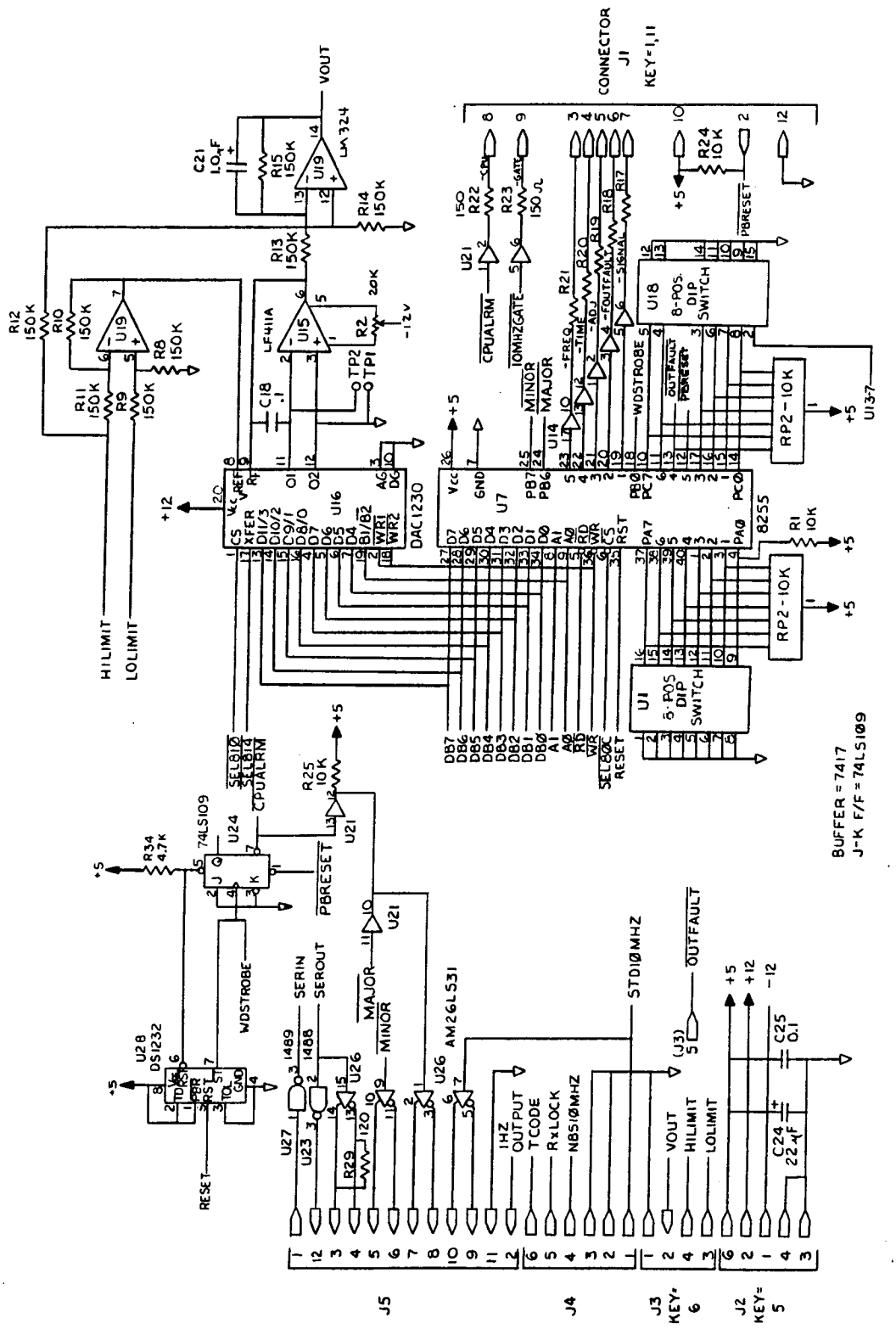


FIGURE 4-11 FTC A6 SCHEMATIC DIAGRAM
SHEET 2 OF 2

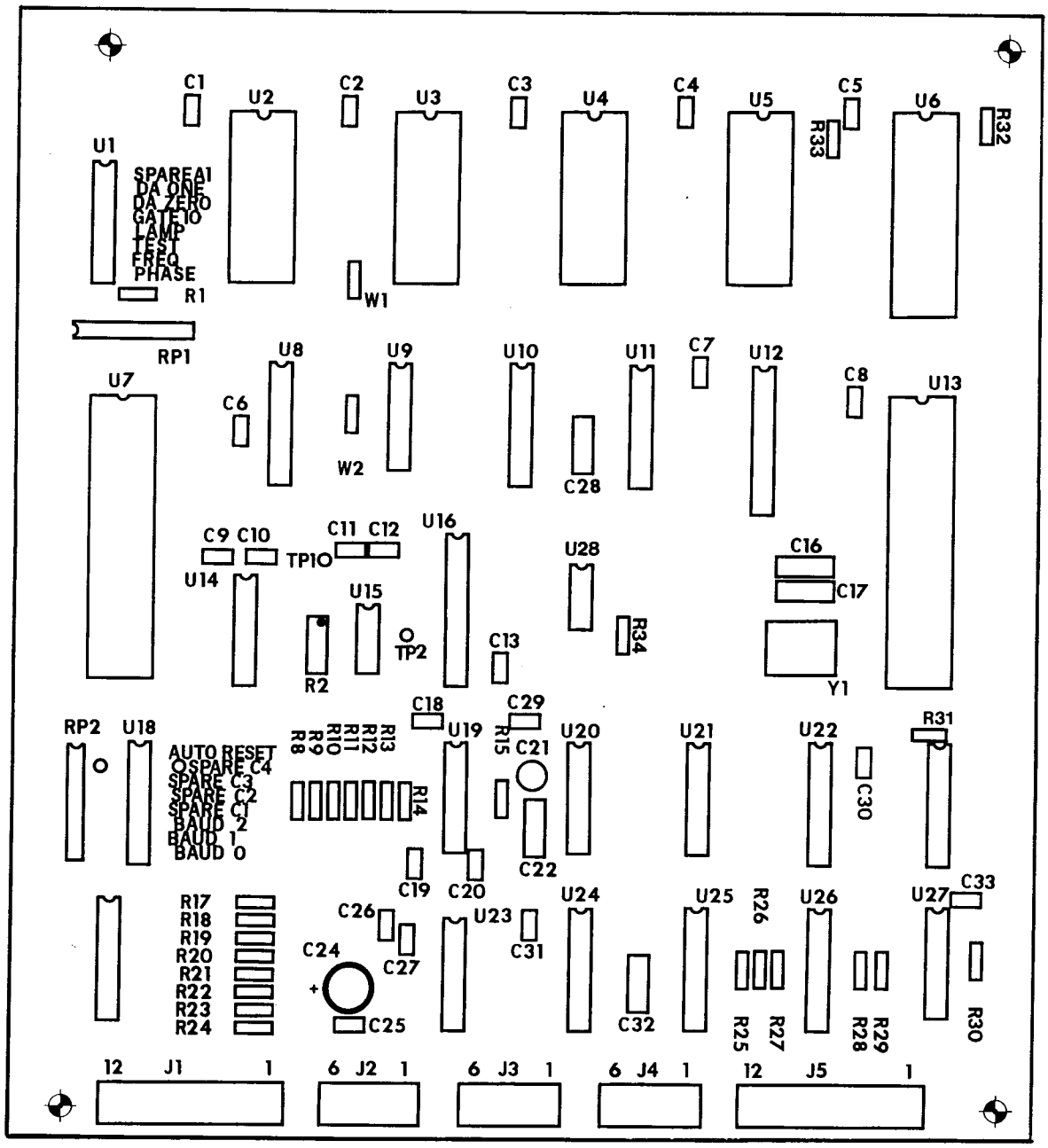


FIGURE 4-12 FTC A6 COMPONENT LOCATION DIAGRAM

4.5.1 Central Processor

The Central Processor portion of the FTC consists of: the 8031 microprocessor (U13), an address latch (U12), a Read Only Memory (U6), a Random Access Memory (U5), and an address decoder (U8). The 11.059 MHz crystal serves as the clock for the CPU. The CPU (U13) fetches instructions from the ROM (U6) by latching the low order address in U12, placing the high order address on Pins 21 through 25, and reading the data bus on Pins 32 through 39. The PSEN signal is used to gate the ROM data onto the data bus. The reading and writing of data to/from the RAM (U5) is similarly accomplished; however, the RD signal is used to gate data to the bus and the WR signal is used to latch data from the bus. The peripheral devices used by the CPU for various functional elements are accessed as external RAM by the CPU. Separate addressing of each of these peripheral devices is accomplished through the address decoder (U8). Instructions and data have separate address space. The data space is shared with the peripheral devices. A summary of the address map is provided below:

Instruction Space

0000-1FFF	ROM (U6)

Data Space

0000-07FF	RAM (U5)
0800-0803	8254 Counter/Timer (U4)
0804-0807	8254 Counter/Timer (U3)
0808-080B	8254 Counter/Timer (U2)
080C-080F	8255 Parallel I/O (U7)
0810-0817	DAC1230 D/A Converter (U16)

Internal to the CPU is a UART and associated baud rate generator. This provides for the connection of a teleprinter for logging and control purposes. The baud is set by software based on the switch settings of U18-6 through U18-8. The serial data is output via TXD (U13-11) and converted to RS-232 levels via U23. Incoming serial data is converted from RS-232 levels to TTL levels via U27 and input to the CPU-UART via RXD (U13-10).

There are two interrupt inputs to the CPU: NIST-5MS and PHASE DIFF INTR. The NIST-5MS is the Realtime Clock input which provides software with a time reference. PHASE DIFF INTR indicates each time a phase difference measurement has been completed between the NIST 1-Hz and the STD 1-Hz. This will occur twice per second, once for each half cycle of the NIST 1-Hz and STD 1-Hz.

The CPU directly reads the NISTHIGH (U13-3) and STDHIGH (U13-4) signals from the Phase Difference circuit. The NISTHIGH is high when the NIST-1Hz leads, in phase, the Time Code (TCODE) received from the WWVB receiver for the last sample. The STDHIGH is high when the NIST-1 Hz leads the STD-1Hz for the last sample.

The CPU also reads the TCODE from the WWVB receiver for the purposes of determining the TCODE symbols received. This is input to the CPU at U13-2. The WWVB receiver locked condition is sensed by the CPU at U13-1.

Three outputs are provided by the CPU for Frequency Counter control: GATE (U13-8), LDCONTR (U13-5), and LDSTR (U13-6).

4.5.2 Realtime Clock

The Realtime Clock (RTC) provides time reference information for the frequency counter. The NIST 10-MHz is first divided by two by the J-K F/F (U25). The resultant 5-MHz signal is fed to the 8254 Counter (U2-18) where it is divided by 25,000 to provide a 5-millisecond square wave output at U2-17.

4.5.3 Frequency Counter

The Frequency Counter provides for the measurement of the STD 10- Mhz output frequency. The counter itself consists of an 8254 Counter (U4) with its three internal counting elements in series. The 10-MHz pulses are gated to the counter chain via the dual F/F arrangement of U22. To enable counting, the CPU activates the GATE line (U13-8) to J-K inputs, U22-2 and 3. Synchronous with the leading edge of the RTC, the GATE will be clocked to the outputs, U22-6 and 7. The CPU will hold the GATE open for the desired period, measured in units of 5 milliseconds. When the GATE is closed, the outputs will change with the subsequent leading edge of RTC.

When U22-14 is high and U22-13 is low, the J-K F/F output U22-10, is allowed to toggle with each leading edge of the STD 10-MHz provided to U22-12. The resultant 5-MHz waveform when applied to the three inverters U21 and the EX-OR gate, U9, will cause a 10-MHz series of pulses to be output from U9. A pulse is generated for each transition of U22-10. Their width is defined by the propagation delay of the three inverters plus the added delay imposed by C22. This pulse shaping circuit is included pursuant to the clock shaping requirements of the 8254 when counting at a 10-MHz rate.

The output pulses of U9 are fed to the AND-OR multiplexer, U11-2. The multiplexer enables the three 8254 counters to be cascaded together or connected to the LDSTR (U13-6) output from the CPU. In order to zero the counters before opening the GATE to count the pulses, the CPU must load the counters with zero. The 8254's, however, will not load the zero count until the first clock pulse. To satisfy this requirement, the CPU initializes the counters by placing a high on the LDCONTR line (U13-5) and pulsing the LDSTR (U13-6) line low. This provides the initializing clock pulse. The LDCONTR is then returned low, returning the counters to the cascaded configuration for counting the 10-MHz pulses.

4.5.4 NIST 1-Hz Clock

The NIST 1-Hz Clock is derived by dividing the NIST 10-MHz from the WWVB receiver. The phase of the NIST 1-Hz is continuously adjusted by the CPU to reflect an in-phase relationship with the "on-time" pulse transmitted by WWVB and received by the receiver. The NIST 10-MHz is fed through a J-K F/F (U25) where it is divided by two. The resultant 5-MHz clock is fed to a prescaling divider (U2-9) where it is further divided by 100 to provide a 50-kHz output at U2-10. The 50 kHz is fed to a final divider (U2-15) where it is divided by 50,000 to provide the NIST 1-Hz output at U2-13. The phase is adjusted under software control by periodically adjusting the 50,000 division factor up or down for one cycle of the divider.

4.5.5 Phase Difference Comparator

The Phase Difference Comparator provides for the evaluation of phase differences between NIST 1-Hz/TCODE and NIST 1-HZ/STD 1-Hz.

The comparison between NIST 1-Hz and TCODE is only on the basis of their overall relationship (i.e. leading/lagging). This is accomplished by TCODE clocking a J-K F/F (U10-12) with the NIST 1- Hz as data input (U10-13 and 14). When the F/F output (U10-10) is high, NIST 1-Hz is leading the TCODE sample in phase.

The comparison between NIST 1-Hz and STD 1-Hz includes both the sign (leading/lagging) and the magnitude. The sign is derived by STD 1-Hz clock in a J-K F/F (U10-4) with the NIST 1-Hz serving as the data input (U10-2 and 3). A high at the F/F output, U10-6, indicates that NIST 1-Hz is leading. The magnitude is derived by EX-ORing the NIST 1-Hz and the STD 1-Hz through U9-12 and 13. The resultant output, U9-11, is used as a gate for counter, U3-16, and also as an interrupt to notify the CPU of available measurements. The counter receives 20 microsecond pulses at U3-18. Each time the gate goes high, the count is zeroed and the incoming pulses are counted. When the gate goes low, counting is disabled and the CPU is interrupted. The counter then reflects the magnitude of phase difference in 20 microsecond units.

4.5.6 D/A Converter

The STD 10-MHz oscillator's frequency is voltage controlled under software direction by programming an output voltage (VOUT) to the oscillator through the D/A Converter. The actual voltage range over which the CPU can program the voltage is established by two inputs to the FTC: LOLIMIT and HILIMIT. LOLIMIT serves as the lower voltage limit of adjustment while HILIMIT serves as the higher limit. These two inputs are fed to a differential amplifier (U19-5 through 7) which provides a negative voltage output to the DAC reference (U16-8) equal to the differential between LOLIMIT and HILIMIT. The DAC (U16) is operated in the current mode. The Op Amp (U15) provides for the conversion of the DAC current into a voltage. The current-to-voltage conversion inverts the DAC output providing positive voltages at U15-6. The output of U15 is fed to a differential amplifier (U19-12 thru 14) which provides the VOUT as the differential between the programmed DAC voltage and the HILIMIT. Therefore, when the DAC is at its minimum numeric value, VOUT is equal to HILIMIT and when the DAC is at its maximum numeric value, VOUT is equal to LOLIMIT.

4.5.7 Watchdog Timer

The Watchdog Timer and power monitor functions are performed by U28. Whenever Vcc falls below 4.75 volts, the reset outputs (Pins 5 and 6) become active. The reset signals also become active at power on when Vcc reaches 4.75 volts.

As part of the FTC software U7-18 provides the periodic pulses, WDSTROBE, to the strobe input U28-7. If a pulse is not received by U28-7 within 1.2 seconds, the last strobe the reset outputs will become active. When this occurs the CPU alarm lamp will be latched on by F/F U24. Depressing the pushbutton reset will clear the CPU alarm.

4.5.8 *Miscellaneous I/O*

There are a variety of miscellaneous I/O signals provided for by the parallel I/O interface, U7, and the open-collector buffers, U14 and U21. These signals fall into three categories: status inputs, status outputs, and switch options.

There are two status inputs: an oscillator output fault indication (OUTFAULT) and a pushbutton status reset (PBRESET). OUTFAULT is introduced to the FTC to indicate a failure in the standard output. It is sampled at U7-13. A low level indicates a fault. The PBRESET is sampled at U7-12. A low level will cause alarm lamps to be reset under software control. This signal is also presented to U24-1 to reset the CPUALRM F/F.

The FTC provides a number of status output indicators. The front panel alarm indicators include: CPU, SIGNAL, OUTPUT, ADJ OSC, and FREQ. The CPU Alarm is directly derived from the CPUALRM F/F (U24) and is buffered by U21 at Pin 1 for open collector output on Pin 2. SIGNAL, OUTPUT ADJ OSC, and FREQ are all derived by software and output via U7 Pins 19 through 23, respectively.

These outputs are buffered by U14 with open collector outputs and current limiting resistors. Rear panel indicators include: MAJOR Alarm and MINOR Alarm. Both of these signals are derived by software and output via U7 Pins 24 and 25, respectively. The MAJOR Alarm is wire-ORed with the CPUALRM via U21 Pins 10 and 12. U26 provides RS-422 level outputs for MAJOR and MINOR alarms.

The FTC includes a number of option switches which enable the user to control various operational characteristics of the FTC through its software. These switches (U1 and U18) are input to U7. Resistor packs, RP1 and RP2, serve as pull-ups. The FTC response to each of these switches is under the control of the software.

Note: U18-1 and 2 are not input to U7.

MODEL 8165

SECTION 5

OPTIONS AND ACCESSORIES

OPTIONS AND ACCESSORIES

5.0 INTRODUCTION

This section describes the following options and accessories that are available for the Model 8165.

* Distribution Amplifier - Option 03
* Line Taps - Model 8140T and 8140TTL
* Line Extender Amplifier - Model 8140TA
* VersaTap™ Frequency Synthesizer Model 8140VT
* MultiTap - Model 8140MT
* DC Input Options 52, 53, and 54
* 10 Hz Channel Offset - Option 31
* External DC Oven Power - Option 55
* Optional Simulcast Offsets - Option 56

Slides (Option 11), the antennas (Model 8206A and Model 8208), and preamplifier (Model 8207) are described in Section 1.

5.1 OPTION 03 BUILT IN DISTRIBUTION AMPLIFIER

Option 03 allows counters and synthesizers throughout a facility to use the WWVB disciplined outputs from a Model 8165 as a common time base. Because equipment can share a common time base, there is no need to buy expensive, high stability time bases for each instrument or remove them from service for periodic calibration.

Units equipped with Option 03 may drive up to 25 remote stations. Multiple outputs are provided on the rear panel so that signals may be sent in several different directions. A line tap at each remote station receives DC power and the 10-MHz from the main coaxial trunk line cable. The signal is buffered then divided to the frequency needed at that station. After filtering, the signal is available at the line tap output. New stations are easily added to the system by inserting additional line taps.

5.1.0 System Components

A frequency distribution system may use Model 8140T or 8140TTL Line Taps, Model 8140VT VersaTap™ or an 8140TA Line Extender Amplifier. The following paragraphs describe each of these units.

5.1.0.1 Model 8140T and Model 8140TTL Line Taps.

These devices, powered by DC on the coaxial feedline, are attached to the coaxial distribution network and provide an output at one of 3 specified frequencies: 1, 5, or 10 MHz. The frequencies of 500 and 100 kHz are available at somewhat higher costs.

Input: Buffered high input impedance causes negligible mismatch on main trunk line distribution cable. Accepts signal levels provided by the base station equipped with Option 03.

Output Level: Standard unit (Model 8140T) provides 600 mV rms sinewave into 50 ohms. When used without termination, the output is TTL compatible. Optional unit (Model 8140TTL) provides TTL 3.4 V rectangular positive pulses from a 50-ohm source.

Output Frequencies: 10, 5.0, 1.0, 0.5 or 0.1 MHz. Specify frequency for each Line Tap ordered.

Harmonic Distortion of Output: -40 dB for standard unit with sinewave output.

Crosstalk (Isolation): 80 dB minimum.

Output Phase Noise: Typically less than -130 dB/Hz 1 kHz from carrier for 10 MHz input to base station amplifier.

Line Tap Size: In inches - 5.25 L x 2.63 W x 1.71 H. (In mm: 133 L x 67 W x 43 H). Mounting hole pattern: 4.75 x 1.75 inches (121 x 44 mm).

Each line tap bears a label showing its output frequency. Should this label be lost, the frequency can easily be determined using a frequency counter or oscilloscope.

5.1.0.2 Model 8140VT VersaTap™ Frequency Synthesizer

The VersaTap™ is a single-frequency synthesizer whose output is factory-set to any frequency between 1 kHz and 16 MHz in 1-kHz increments and up to 20 MHz in 2 kHz increments. Some special frequencies can be furnished, such as the 3.5795454...MHz TV color sub-carrier. Exact frequencies must be specified at time of order.

Input: Buffered high impedance input. Accepts 10.0 MHz with signal level between 100 millivolts and 5.5 Vp-p on a DC voltage of 7 to 12 VDC. The DC current requirement is 110 milliamps at +12 VDC.

Output A: A sinewave of 600 mV rms at the specified frequency into a 50-ohm load for frequencies greater than 100 kHz. A TTL output for frequencies below 100 kHz with a source impedance of 50 ohms (SN74S140) driver.

Output B: A TTL output at the specified frequency with a source impedance of 50 ohms (SN75S140 driver). If the internal jumper, W6, is moved to location W5, Output B is HIGH when the

VersaTap™ is phase locked to the incoming reference and LOW when it is unlocked.

Lock LED: The LED will light when the VersaTap™ is locked to the incoming reference. The LED will blink if the DC input is low, which may cause the VersaTap™ to malfunction. The LED will be unlit when the VersaTap™ is not locked to the incoming reference.

VersaTap™ Size: In inches 8.3 L x 4.2 W x 1.7 H. (In mm: 211 L x 107 W x 43 H). Mounting hole pattern 8.88 x 2.75 inches (225.4 x 69.9 mm).

5.1.0.3 Model 8140TA Line Extender Amplifier

The Line Extender Amplifier must be used to boost the output signal when the coaxial distribution network is more than 1500 feet (457 m) long. The Line Extender will drive an additional 1500-feet (457 m) of RG58 coaxial cable with Model 8140 Line Taps installed along its length.

Two DC-isolated 50-ohm terminators must be used: one at the input tee connector of the Line Extender Amplifier and one at the far end of the cable connected to the output of the Line Extender Amplifier.

See the "Typical Interconnection Diagram" at the end of this section for an approved method of interconnection.

5.1.0.4 Model MultiTap

The Spectracom Model 8140MT MultiTap is a programmable frequency divider/buffer. Three outputs can be configured to the same frequency or set independently. When used as part of your Spectracom Distribution System it decreases the cost per output and allows future modifications as requirements change.

Frequency Outputs: Three square wave outputs per MultiTap. 1.5V p-p into 50 ohms. Once group is chosen, any divisor in a group may be individually selected.

Table of output divisors:

Group A	B	C	D
1	1	5	5
2	2	10	10
10	20	50	100
50	100	250	500
250	500	1250	2500

For a 10-MHz input, the available outputs in MHz are:

Group A	B	C	D
10.0	10.0	2.0	2.0
5.0	5.0	1.0	1.0
1.0	0.5	0.2	0.1
0.2	0.1	0.04	0.02
0.04	0.02	0.008	0.004

Power Requirements: When driven by a Distribution Amplifier, the DC load equals 3 line taps. Option 40, which is required for stand-alone operation, reduces the distribution load to 1 line tap equivalent, and is required whenever output frequencies are below 100 kHz. Maximum current is less than 150 mA.

MultiTap size: 5.25L x 2.63W x 1.71H in. (133L x 67W x 43H mm)

Mounting hole: 4.75 x 1.75 in. (121 x 44 mm)

5.1.1 Design of Distribution Networks

This section provides guidelines for using the Option 03 distribution outputs. In planning a system installation follow the guidelines listed below:

1. A maximum of 25 line tap loads may be driven from one base station. More than 25 loads is not permitted due to power supply limitations and impedance matching. Table 5-1, Line Tap Loads, lists the equivalent number of loads and current each distribution device consumes. The receiver may provide up to 1.2 amps total to the distribution network.

DEVICE	LOADS	CURRENT (mA)
8140T All Versions	1	45
8140TA	1	45
8140VT Standard	3	150
8140VT w/Opt 45	5	250
8140VT w/Opt 48	4	200
8140VT w/Opt 58	4	200
8140MT	3	150

TABLE 5-1 LINE TAP LOADS

If more than 25 line tap loads are required you may:

Add a Model 8140 Frequency Distribution Amplifier. The Model 8140 contains an internal power supply and will feed an additional 25 line tap loads. A line tap is required (typically 10 MHz) to provide the input frequency source to the Model 8140. This "Daisy Chaining" may be continued indefinitely.

2. Because of voltage drops and signal attenuation the longest trunk line using RG-58 cable is 1500 feet (457 m).

   Figure 5-1, Line Tap Number and Distance Chart, is used to calculate the number of line tap loads that may be used at various distances from the base station.

   For example, if 25 line taps are used, their average distance from the amplifier is limited to 750 feet (228 m), using RG-58. Up to 12 line taps may be placed at 1500 feet (457 m) on any one trunk line.

If longer runs are required, you may:

A. Locate the Model 8165 in the geographical center of the installation, running distribution lines in both directions and achieving a coverage of 3000 linear feet (914 m).

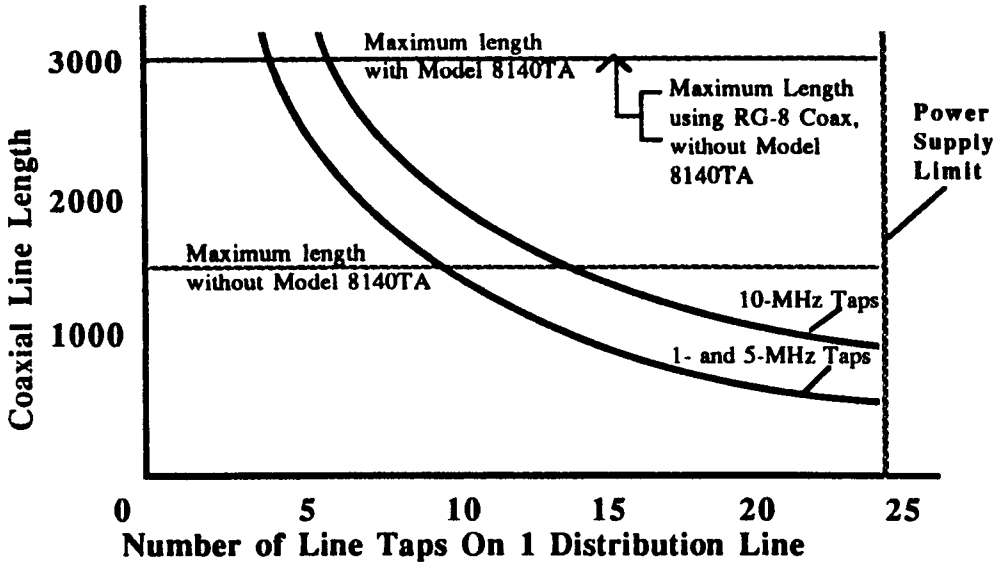


FIGURE 5-1 LINE TAP NUMBER AND DISTANCE CHART - OPTION 03

B. Use a Model 8140TA Line Extender Amplifier at 1500 feet, allowing a further 1500-foot (457 m) extension of the distribution line. The Model 8140TA counts as one line tap towards the total number allowed. Use a Distribution Line Termination, Part Number 004490, at the input tee connector and at the end of the extended line section as shown in the "Typical Interconnection Diagram", Figure 5-2.

C. Use a Model 8140 Frequency Distribution Amplifier.

3. Each distribution line must be continuous from the base station to the DC isolated 50 ohm load that must be used at the far end. Line taps are inserted along the distribution line by using the supplied input tee connector. No branching or "Y" configurations may be used as this causes impedance mismatch on the line. Anything other than a 50 ohm line impedance may cause reflections which can cancel the output waveform at the receiver triggering the output fault lamp. Refer to the Typical Interconnection Diagram, Figure 5-2 for an approved method of interconnection.

4. Five DC-isolated 50 ohm loads are furnished with each unit equipped with Option 03. They may be found in the ancillary kit that is packed with each unit when it leaves the factory. If any of these loads are lost, spares may be purchased from Spectracom. The part number to order is 004490. Terminators may be placed on any unused distribution output connector to prevent loss.

5. We recommend that, wherever practical, the line taps be permanently mounted to a lab bench or wall nearby. This avoids their loss or misplacement and discourages people from occasionally disconnecting them, thus cutting off the signal to stations further down the line.

6. Never directly connect a distribution line to an instrument; always use a line tap or VersaTap™. Doing so may damage the instrument or cause an impedance mismatch on the distribution line.

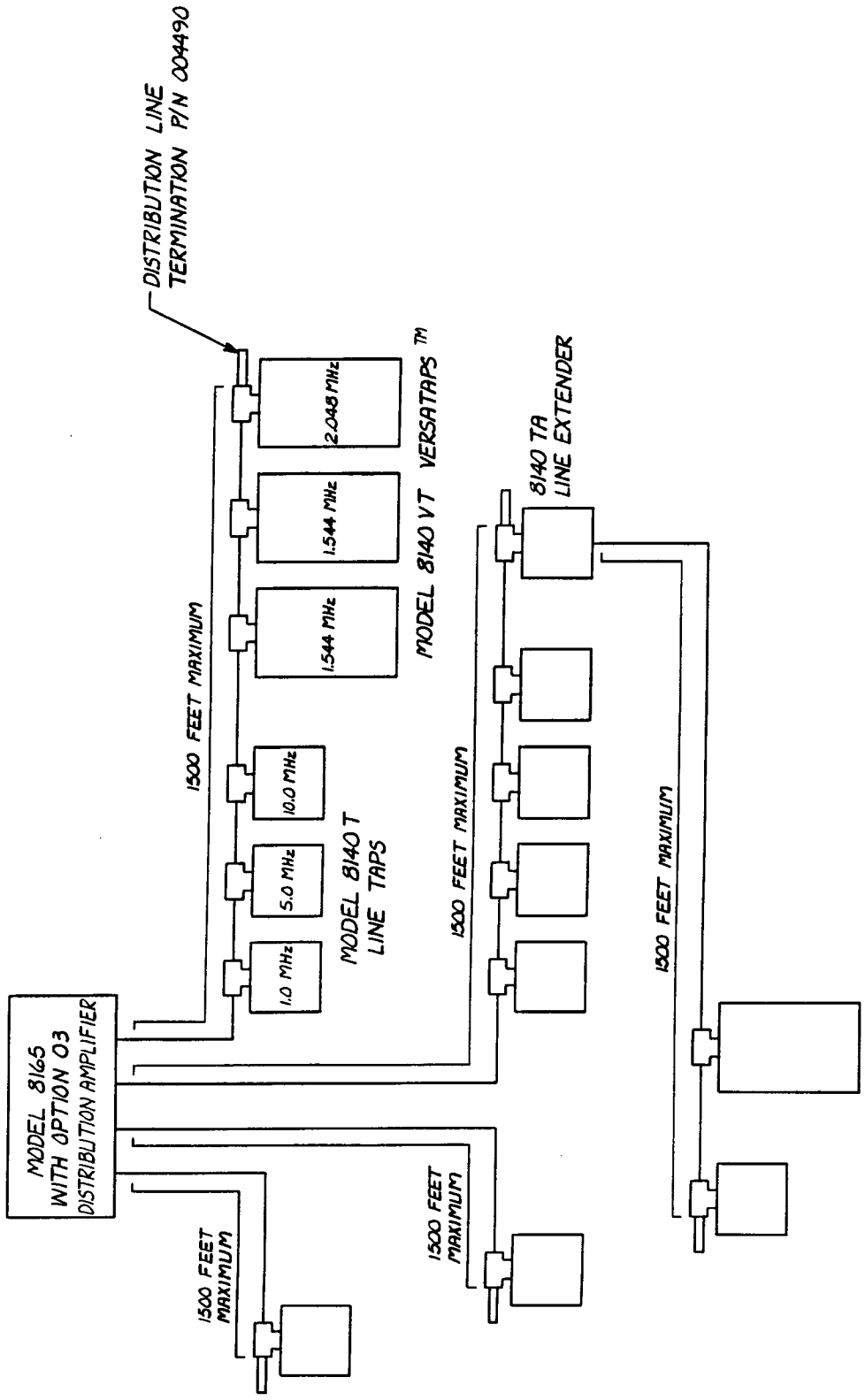


FIGURE 5-2 TYPICAL INTERCONNECTION DIAGRAM

5.2 OPTION 31 - 10-HZ CHANNEL OFFSET

To avoid interference between TV stations operating on the same frequency, geographical separation and radiated powers are carefully selected. Nevertheless, considerable co-channel interference has been encountered.

Co-channel interference between TV stations appears to viewers as a horizontal pattern of alternating light and dark bars much like the shadows cast by venetian blinds. The visibility of these bars varies cyclically as a function of the difference frequency of the interfering carriers.*1*

Co-channel interference can be minimized if the transmitter frequencies are tightly controlled. To minimize the interference, the visual carrier of an interfering station is offset by either plus or minus 10,010 Hz. The 10-kHz offset and the direction (i.e. plus or minus) is assigned by the FCC. This offset is normally provided in the transmitter. The Model 8165 Disciplined Oscillator with Option 31 provides a precise 10-MHz standard with offset control that, when translated to the visual carrier frequency results in an additional 10 Hz offset.

5.2.0 Frequency Offsets

The internal dip switches A6U1-1 labeled Spare A1 and A6U18- 2,3,4,5 labeled Spare C4, Spare C3, Spare C2, and Spare C1, control the 10-MHz offset. Table 5-2 FREQUENCY OFFSET TABLE, lists the frequency as a function of switch setting for each of the VHF-TV channels.

1 "Precise Frequency Control, Theory and Practice" by J.L. Klecker and A.H. Bott, Engineering Report, Harris Corporation, Broadcast Division, 123 Hampshire Street, Quincy, Illinois 62301.

CHANNEL	SWITCH A6U18 -2 -3 -4 -5 C4 C3 C2 C1	FREQUENCY - HZ PLUS OFFSET A6U1-1 = ON	MINUS OFFSET A6U1-1 = OFF
X	0 0 0 0	10,000,000.000	10,000,000.000
X	0 0 0 1	10,000,000.000	10,000,000.000
2	0 0 1 0	10,000,001.810	9,999,998.190
3	0 0 1 1	10,000,001.632	9,999,998.367
4	0 1 0 0	10,000,001.487	9,999,998.513
5	0 1 0 1	10,000,001.294	9,999,998.706
6	0 1 1 0	10,000,001.201	9,999,998.799
7	0 1 1 1	10,000,000.571	9,999,999.429
8	1 0 0 0	10,000,000.552	9,999,999.448
9	1 0 0 1	10,000,000.534	9,999,999.466
10	1 0 1 0	10,000,000.517	9,999,999.483
11	1 0 1 1	10,000,000.502	9,999,999.498
12	1 1 0 0	10,000,000.487	9,999,999.513
13	1 1 0 1	10,000,000.473	9,999,999.527
XX	1 1 1 0	10,000,000.000	10,000,000.000
XX	1 1 1 1	10,000,000.000	10,000,000.000

SWITCH A6U1 & A6U18
1 = ON; 0 = OFF

TABLE 5-2 FREQUENCY OFFSET TABLE

For TV Channel 2 with a plus 10-kHz offset, place A6U1-1 Spare A1 and A6U18-4 Spare C2 in the ON position and A6U18-2,3 and 5 in the OFF position. This selects a frequency of 10,000,001.810 Hz for the 10-MHz standard, providing an additional 10-Hz offset at visual carrier frequency.

When shipped from the factory, the unit is set to the frequency specified on the rear panel label. If a different selection is required, remove the top cover and select the new frequency.

The frequency correction switch, A6U1-7, must be on to allow the unit to frequency lock. An offset may be entered without removing power. Once an offset is entered a FREQ alarm occurs causing a major alarm. A major alarm removes the rear panel outputs if the signature control feature is enabled. The outputs will return when the unit synchronizes to within 1 x 10^{-8} of the expected frequency. Once this occurs the FREQ and OUTPUT lamps are cleared by depressing the RESET button.

5.2.1 Performance

The Model 8165 operates on a "frequency locking" principal. The frequency of the 10-MHz standard oscillator is measured and control voltage corrections applied to bring it to the desired frequency. The time base for the measurement is derived from the received WWVB signal. The measurement interval is 1000 seconds. The measurement resolution is one part in 10 to the 10th power (1×10^{-10}). The standard frequency is measured and a correction voltage is computed to bring the standard to the desired frequency. The adjustment resolution is 2.4 parts in 10 to the 10th power (2.4×10^{-10}). The long term accuracy is typically plus or minus one part in 10 to the 9th power (1×10^{-9}). The frequency offsets may be verified by the Offset Performance Test described in Section 6.

5.3 DC INPUT OPTIONS

DC Input Options allow the Model 8165 to operate from a DC voltage source. The DC power connection is made at the **DC INPUT** terminal block. The optional input voltages are listed below:

OPTION 52	±13.8 VDC ±20% (±12 VDC) 25 WATTS
OPTION 53	±27.6 VDC ±20% (±24 VDC) 25 WATTS
OPTION 54	±55.2 VDC ±20% (±48 VDC) 25 WATTS

The isolated inputs of the DC-DC converters permits either polarity of voltage to be used.

NOTE: Be certain to observe the **DC INPUT** polarity markings. Reversing connections will result in a blown **DC** fuse.

The DC-DC power supply provides +27 V for oscillator operation, +5 V for Logic and ±15 V for regulation to ±12 V. Figure 5-3 shows the DC input options wiring connections. Refer to Figures 5-4 and 5-5 for the schematic and component location diagrams of the DC-DC power supply board.

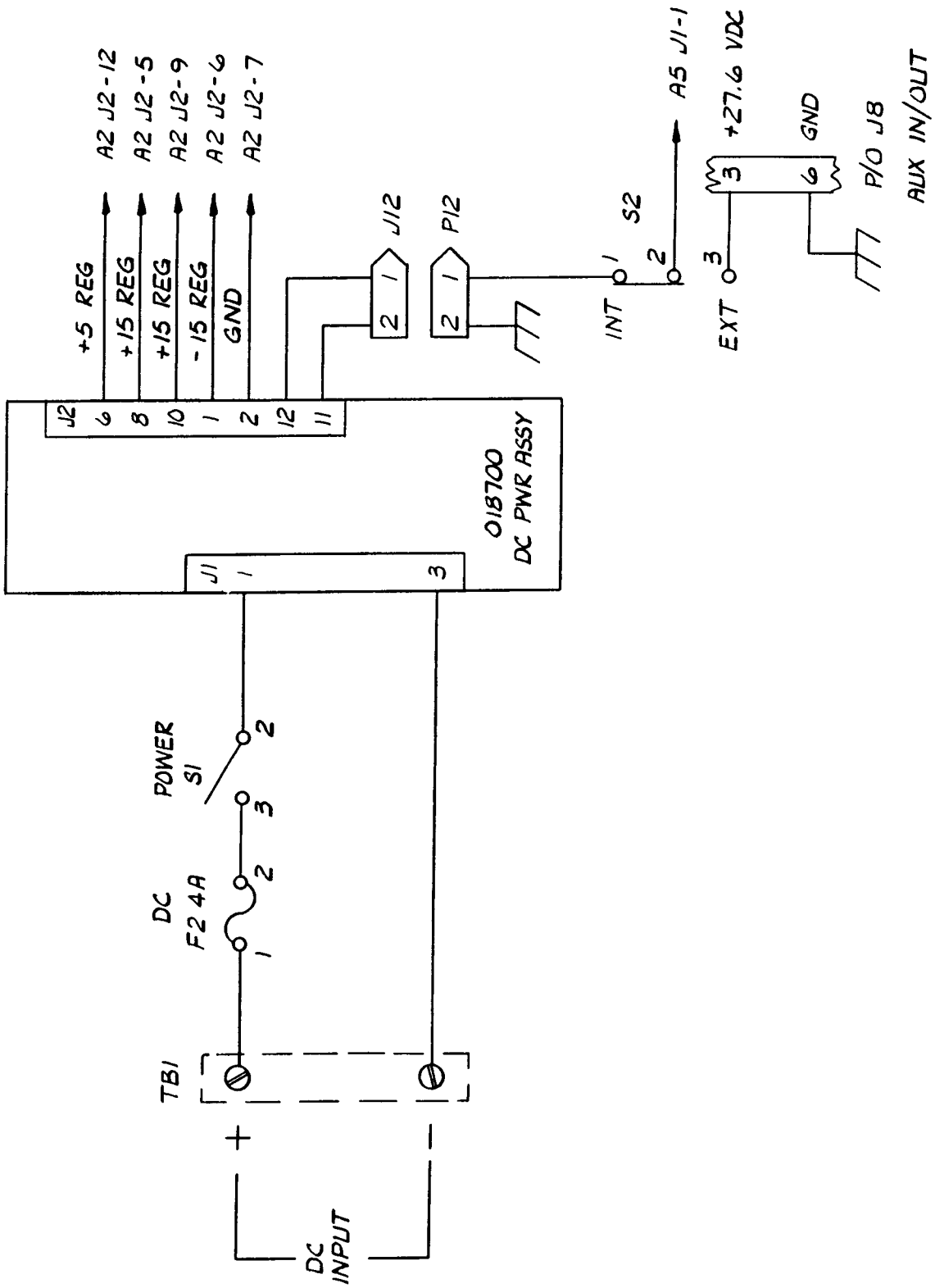


FIGURE 5-3 DC INPUT MAINFRAME SCHEMATIC DIAGRAM

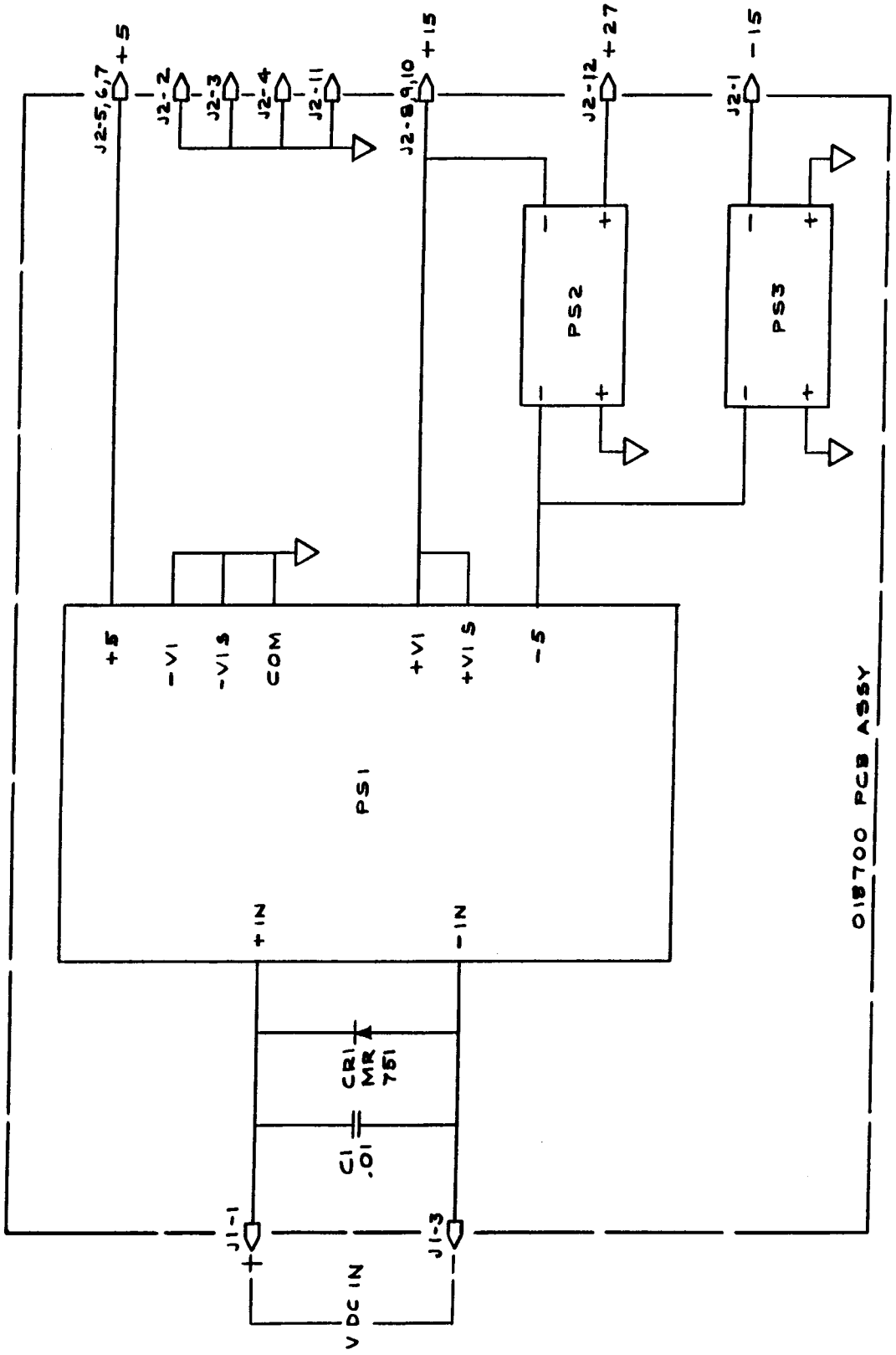


FIGURE 5-4 DC INPUT SCHEMATIC DIAGRAM

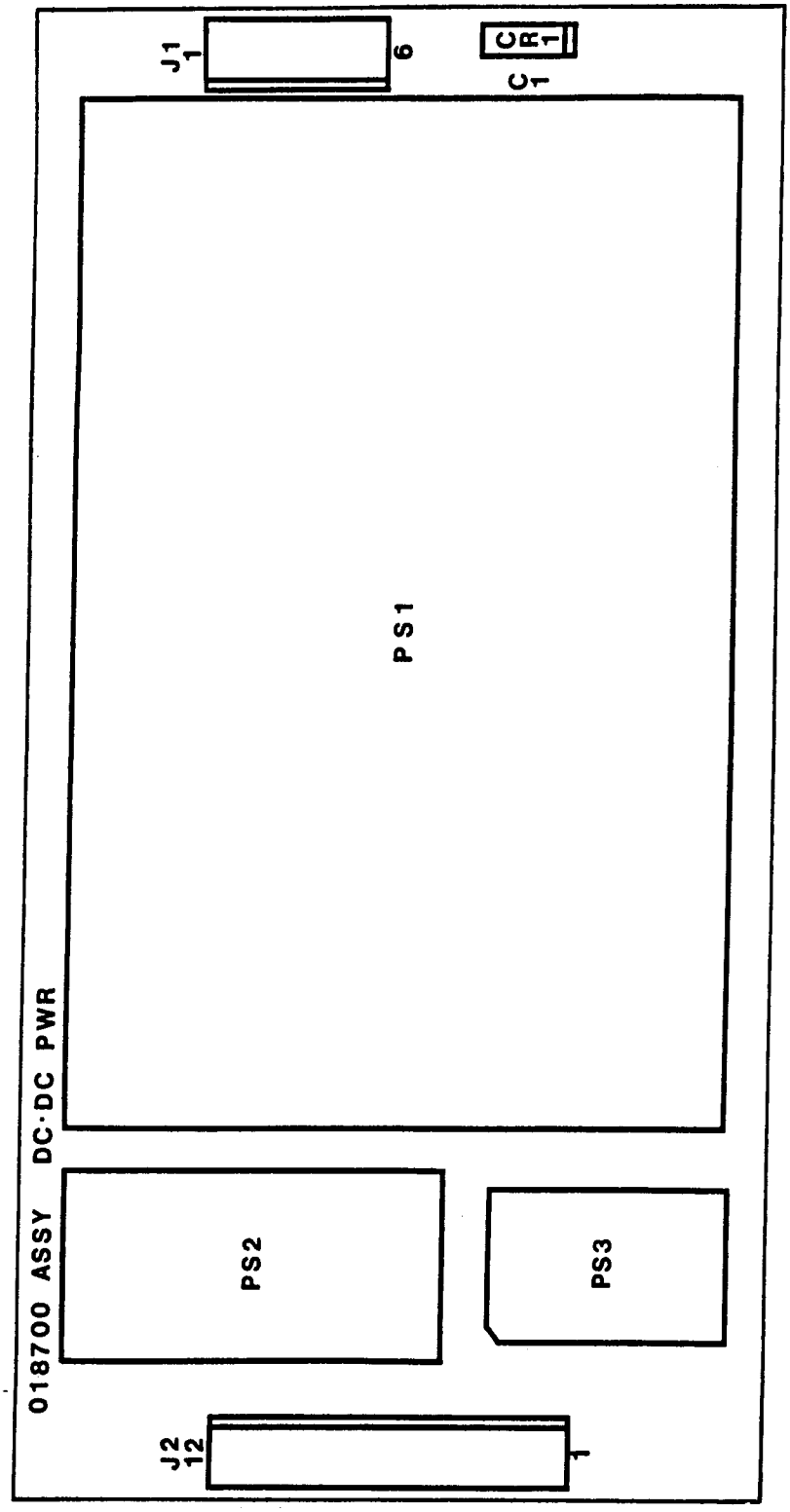


FIGURE 5-5 DC INPUT COMPONENT LOCATION DIAGRAM

5.4 OPTION 55 EXTERNAL DC OVEN POWER

This option replaces the internal battery with a DC-DC converter to allow oven standby from an external DC power bus. The input is ±27.6 VDC ±20% (±24 VDC). Power connection is made at the **DC INPUT** terminal block. Either polarity may be used due to the isolated input of the DC-DC converter. The oven DC switch must be in the OP55 position. Figure 5-6 shows the Option 55 wiring connections diagram. Refer to Figures 5-7 and 5-8 for the Option 55 Schematic and PC Board Assembly.

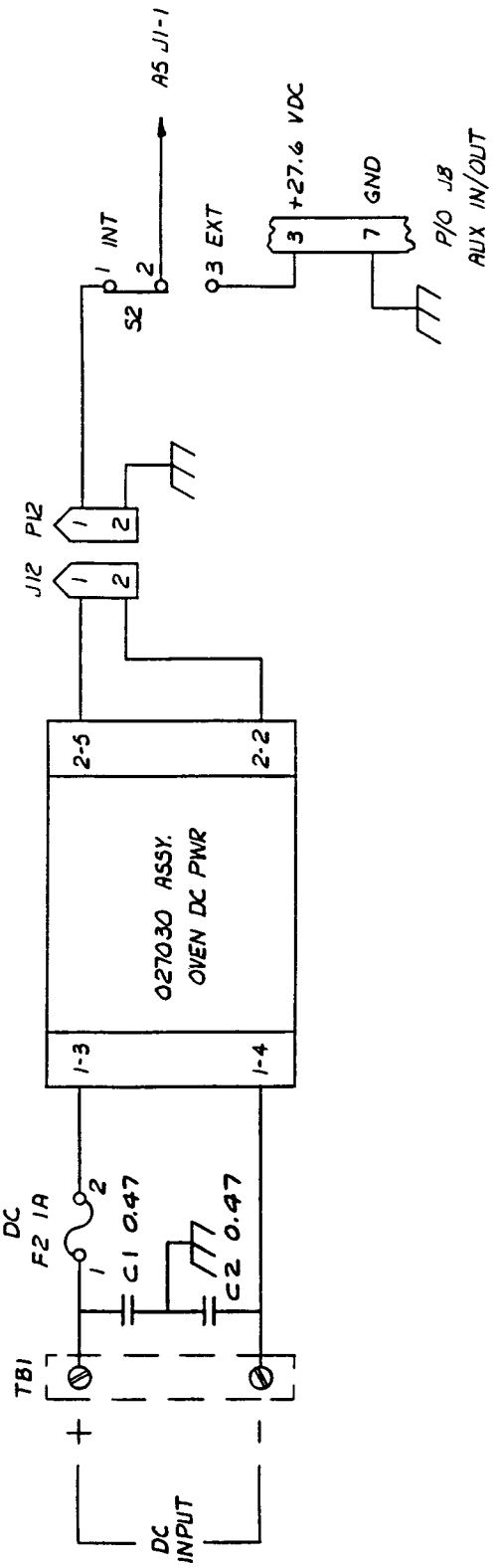


FIGURE 5-6 OPTION 55, MAINFRAME SCHEMATIC DIAGRAM

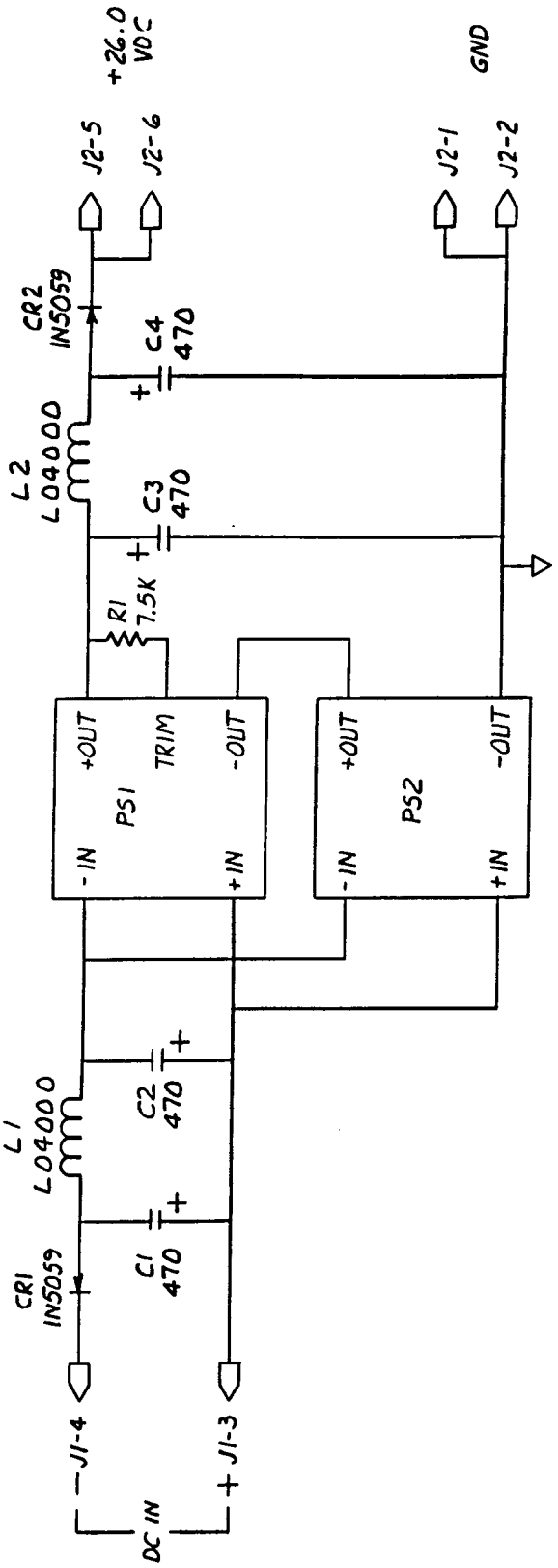


FIGURE 5-7 OPTION 55 DC-DC CONVERTER SCHEMATIC DIAGRAM

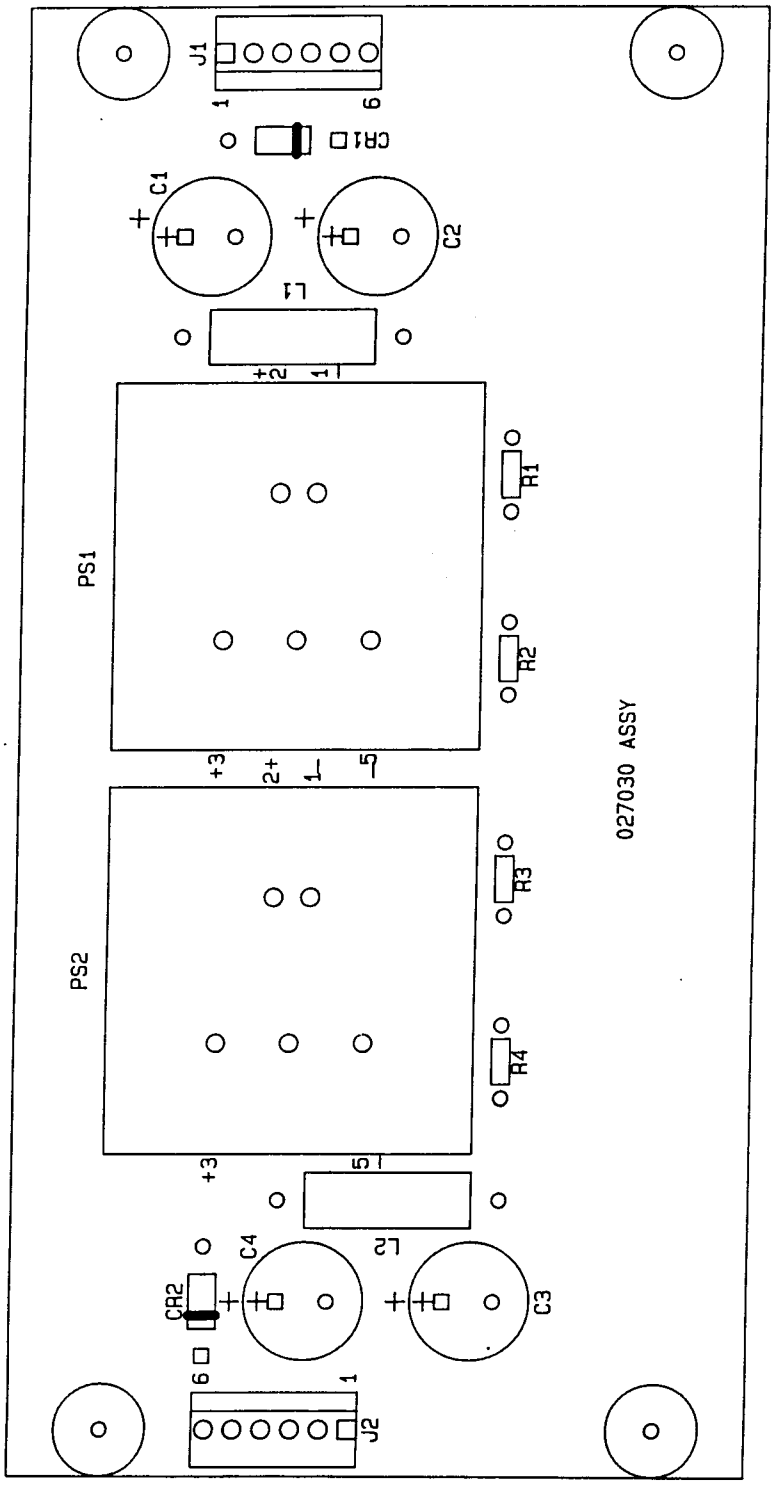


FIGURE 5-8 OPTION 55 DC-DC CONVERTER COMPONENT LOCATION DIAGRAM

5.5 OPTIONAL SIMULCAST OFFSETS

Option 56 allows the 10-MHz standard to be offset in smaller step sizes than the standard simulcast offsets. The standard simulcast format offsets the 10-MHz standard 6.62 x 10^{-9} per step. Option 56 decreases the step size to 1.11 x 10^{-9} per offset step. The effect of the smaller step size when multiplied up to the carrier frequency is shown in Table 5-3.

	APPROX OFFSET STEP SIZE		
	VHF	UHF	800 MHz
STANDARD	1.0 Hz	3.0 Hz	5.3 Hz
OPTION 56	0.17 Hz	0.5 Hz	0.9 Hz

TABLE 5-3 SIMULCAST OFFSET STEP SIZE

5.5.0 Frequency Offsets

A frequency offset is entered into the Model 8165 by dip switches A6U1-1 and A6U18-2,3,4,5. Table 5-4, Frequency Offsets, lists the frequency of the 10-MHz standard as a function of switch settings. The positive offset column shows that for Channel 0, a precise 10.0-MHz frequency is provided. For Channel 1, the frequency is 10,000,000.011 Hz. For Channel 15, the frequency is 10,000,000.166 Hz.

NOTE: Offset is positive when A6U1-1 is on, and offset is negative when A6U1-1 is off.

Offset Step	Switch A6U18 -2 -3 -4 -5 C4,C3,C2,C1	Frequency (in hertz) Positive Offset A6U1-1 = ON	Relative Negative Offset A6U1-1 = OFF	Frequency Δf_S
0	0000	10,000,000.000	10,000,000.000	0.0
1	0001	10,000,000.011	9,999,999.989	1.1×10^{-9}
2	0010	10,000,000.022	9,999,999.978	2.7×10^{-9}
3	0011	10,000,000.033	9,999,999.967	3.3×10^{-9}
4	0100	10,000,000.044	9,999,999.956	4.4×10^{-9}
5	0101	10,000,000.055	9,999,999.945	5.5×10^{-9}
6	0110	10,000,000.066	9,999,999.934	6.6×10^{-9}
7	0111	10,000,000.077	9,999,999.923	7.7×10^{-9}
8	1000	10,000,000.088	9,999,999.912	8.8×10^{-9}
9	1001	10,000,000.099	9,999,999.901	9.9×10^{-9}
10	1010	10,000,000.111	9,999,999.889	11.1×10^{-9}
11	1011	10,000,000.122	9,999,999.878	12.2×10^{-9}
12	1100	10,000,000.133	9,999,999.867	13.3×10^{-9}
13	1101	10,000,000.144	9,999,999.856	14.4×10^{-9}
14	1110	10,000,000.155	9,999,999.845	15.5×10^{-9}
15	1111	10,000,000.166	9,999,999.834	16.6×10^{-9}

TABLE 5-4 FREQUENCY OFFSETS

The frequency correction switch, A6U1-7, must be on to allow the unit to frequency lock. An offset may be entered without removing power. Once an offset is entered a FREQ alarm occurs causing a major alarm. A major alarm removes the rear panel outputs if the signature control feature is enabled. The outputs will return when the unit synchronizes to within 1 x 10^{-8} of the expected frequency. Once this occurs the FREQ and OUTPUT lamps are cleared by depressing the RESET button.

5.5.1 Frequency Offset at the Carrier Frequency

The frequency offset at the carrier frequency is determined by for formula:

$$\Delta f_c = F_c \times \Delta f_s$$

where:

Δf_c = carrier offset

F_c = carrier frequency

Δf_s = offset of 10 MHz standard (from Table 2-2)

Table 5-5, Offset at 450 MHz carrier frequency, lists the frequency offset in Hertz as a function of switch setting.

NOTE: Offset is positive when A6U1-1 is on, and negative when A6U1-1 is off.

Offset Step	Switch A6U18 -2 -3 -4 -5 C4,C3,C2,C1	Offset (in Hertz) at 450 MHz
0	0000	0.0
1	0001	0.5
2	0010	1.0
3	0011	1.5
4	0100	2.0
5	0101	2.5
6	0110	3.0
7	0111	3.5
8	1000	4.0
9	1001	4.5
10	1010	5.0
11	1011	5.5
12	1100	6.0
13	1101	6.5
14	1110	7.0
15	1111	7.5

TABLE 5-5 OFFSET AT 450 MHz CARRIER FREQUENCY

5.5.2 Performance

The frequency offsets may be verified by the Offset Performance Test described in Section 6 of this manual.

MODEL 8165

SECTION 6

SERVICE INFORMATION

SERVICE INFORMATION

6.0 INTRODUCTION

This section contains information on calibration and performance testing of the Model 8165. Included in this section are Accessory Tests and Troubleshooting.

6.1 TEST EQUIPMENT

Table 6-1 lists the recommended test equipment for checking the performance of the Model 8165.

Test equipment with equivalent characteristics may be substituted.

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED
WWVB Antenna	60 kHz Active Antenna	Spectracom Model 8206
Oscilloscope	2-channel	Tektronix Model 455
Voltmeter	4-1/2 Digit Multimeter	Data Precision Model 255
Counter	Accuracy $\pm 1 \times 10^{-7}$	HP 5315B Universal Counter
Signal Generator	60 kHz, $\pm 1 \times 10^{-7}$ Accuracy. Output less than 0.2 μV.	Marconi Model 2022
Data Terminal	RS-232C Interface	Teletype Model 43 300 Baud

TABLE 6-1 RECOMMENDED TEST EQUIPMENT

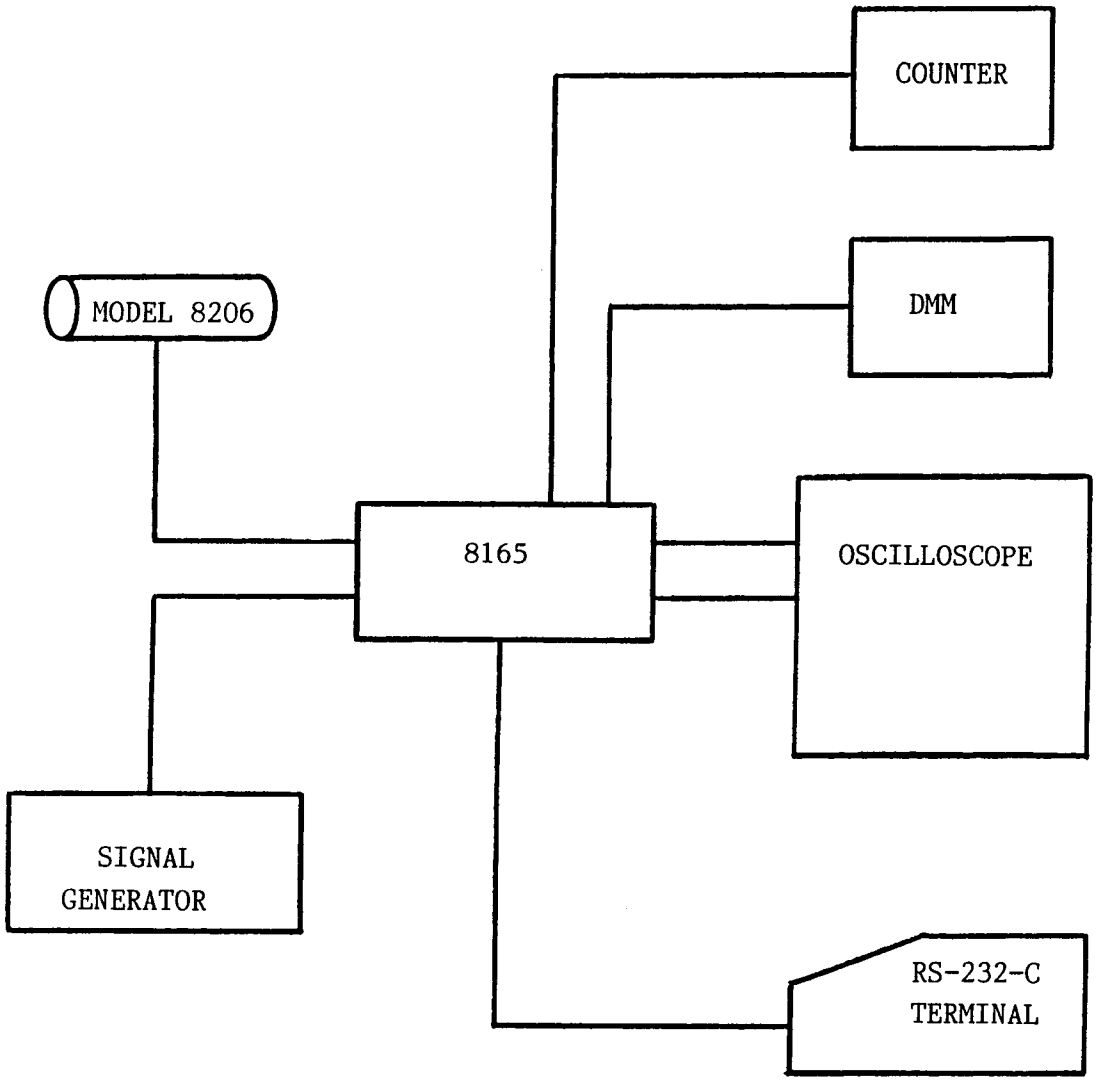


FIGURE 6-1 TEST SET-UP

6.2 BENCH SET-UP

Figure 6-1 shows the test set-up. The signal generator is used to simulate the 60 kHz signal transmitted by WWVB.

CAUTION: There is 12 VDC at the antenna input connector. This is used to power the Model 8206A Loop Antenna or the Model 8207 Line Preamplifier. It may be necessary to connect a decoupling capacitor between the signal generator and receiver if the generator is not reverse power protected. If needed, choose a capacitor value around 10 μF and install with the plus side (+) to the receiver.

6.3 PERFORMANCE CHECKS

6.3.1 Power Supplies

This test checks the power supply voltages.

+5 Volts	(±.25) A2J3-1	_____V
+12 Volts	(±0.5) A2J4-4	_____V
-12 Volts	(±0.5) A2J4-1	_____V

6.3.2 RF Amplifier Checks

The purpose of these checks is to verify that input transformer T1 and crystal filter C8, C9, and Y1 have been tuned. The RF Amplifier is designated as the A1 Board. Refer to Figure 4-4 on page 4-6 for the component location diagram.

Disconnect the AGC wire (violet) from connector A2J5, pin 6.

Connect the oscilloscope probe to A2E1. The Receiver Board is designated as the A2 Board. Refer to Figure 4-6 on page 4-11 for the component location diagram.

Set the signal generator and attenuator to provide an unmodulated 1.0 microvolt signal (rms) at exactly 60 kHz.

Apply power to the receiver and adjust the signal generator level to provide a 1 Vp-p output signal on the oscilloscope.

Adjust the slug in the transformer, A1T1, for a peak on the oscilloscope, while reducing the signal generator to maintain a 1 Vp-p output.

INPUT VOLTAGE AT 1 Vp-p OUTPUT_____μV

Adjust capacitor A1C8 for maximum output on the oscilloscope.

TUNE CRYSTAL FILTER A1C8_____

Change the signal generator frequency to 100 KHz and increase the output for a reading of 1 Vp-p at A2E1. During this test do not exceed 0.1 volt rms at the antenna input. Adjust capacitor A1C9 for minimum output on the oscilloscope while increasing the signal generator level to maintain a 1 Vp-p output.

TUNE STOP BAND NULL A1C9_____

Change the signal generator frequency to 60 kHz at a 1 millivolt RMS input level. The output waveform (A2E1) should be a square wave with a 50% ±10% duty cycle and 3 Vp-p ±20%.

OUTPUT SIGNAL A2E1,
50% duty cycle ±10%_____

OUTPUT SIGNAL A2E1
3 Vp-p ±20%_____V

NOTE: This completes the alignment of the RF Amplifier. The AGC potentiometer adjustment is described in TEST 6.3.9.

6.3.3 Quadrature Detector and Phase Detector Balance

This checks the adjustment of potentiometers A2R3 and A2R5. Remove the input signal to the antenna input.

Connect a clip lead from A2E2 to A2E3. Connect the negative lead of the DVM to A2TP3, and the positive lead to A2TP4. Set the DVM to ±2V full scale. Make no connection to the antenna input.

Apply power to the receiver and adjust A2R30 for a zero reading on the DVM. Slight digit changes may be noticed, but should be less than ±5 mV. Move the positive DVM lead from A2TP4 to A2TP6. The reading should be less than ±500 mV.

QUAD DETECTOR BALANCE_____

Connect the negative DVM lead to A2TP1 and the positive lead to A2TP2. Adjust A2R5 for a zero reading on the DVM. Changes of ±5 mV or less may be noticed.

PHASE DETECTOR BALANCE_____

6.3.4 Lock Volts Adjust

This test adjusts A2R14. Move the clip lead from A2E3 to A2E4. Connect the DVM between GND and A2J1 Pin 10 to read lock volts. Adjust A2R14 for a meter reading of 2.16 volts. Glyptol A2R14.

LOCK VOLTS (2.16 volts)_____

6.3.5 *Oscillator Adjust*

Connect the frequency counter to the 10-MHz phase locked output at A2J1-13. Adjust A2C10 for a counter reading of 9,999,900 Hz.

OSCILLATOR PRESET (9,999,900 Hz)_____Hz

6.3.6 *Oscillator Symmetry*

Disconnect the clip lead from A2E2 to A2E4. Reconnect an oscilloscope to A2J1-13. Adjust A2R23 so the 10-MHz signal is a symmetrical square wave. Glyptol A2R23.

OSCILLATOR SYMMETRY_____

6.3.7 *Final Adjust 10-MHz Oscillator*

Adjust the signal generator to 60.000 kHz unmodulated and 1 mV rms when connected to the receiver antenna. The receiver should lock, indicated by a green lock light and a lock voltage near 1.4 VDC. Adjust A2C10 very slowly until the lock voltage is 1.40 VDC.

LOCK VOLTS A2J1-10 (1.40 VOLTS)_____

6.3.8 *Final Adjust Phase Detector Balance*

Disconnect the signal generator from the antenna and note the lock voltage drift. Disregard any sudden small jump at the moment of disconnect. If a downward drift is observed then turn A2R5 clockwise by very small amounts until the drift is stopped. Small jumps may occur as A2R5 is adjusted. Disregard these and note only the slow drift. If an upward drift is observed, then turn A2R5 counterclockwise by very small amounts. This is a very fine adjustment and is completed when no perceptible drift is evident after one minute of observation. Glyptol A2R5.

6.3.9 *AGC Voltage Control Adjust A1R19*

Connect the negative lead of the DVM to A2TP3 and the positive lead to A2TP6. Adjust the signal generator to 60.000 kHz and 1 μV when connected to the ANTENNA input. The meter is reading the AGC voltage with the AGC feedback loop open (the AGC wire, A1P2-6, was disconnected during the testing of the RF Amplifier). Lock-up may take several minutes at 1 μV input. The voltage at A2TP6 may continue to rise after the green lock light comes on.

Adjust the signal generator in small amounts (less than 1 dB) until the voltage is approximately +2.38 V. Wait one or more minutes between level changes. The voltage read on the DVM is delayed by a long time constant in the AGC loop. A 2.38 V reading is normally reached with an antenna input level between 0.25 and 1.0 μV.

AGC VOLTS A2TP3 TO A2TP6 (2.38V)_____V

Reconnect the violet AGC wire to A1P2-6. The DVM reading will slowly decrease to a lower value. Adjust the AGC control A1R19 in very small amounts until the DVM stabilizes 1V lower or approximately +1.38V. Because of the long time constant in the AGC loop, wait one or more minutes between adjustments. Glyptol A1R19.

AGC VOLTS A2TP3 TO A2TP6 (1.38V)_____V

6.3.10 Receiver Sensitivity

This test measures the receiver sensitivity. Increase the signal generator level to 10 μV and wait a minute for the receiver to stabilize. Decrease the signal generator level to 1.0 μV and allow one minute for the receiver to stabilize. The green LOCK light should be on. Slowly decrease the signal generator level until the red UNLOCK light comes on. Do not exceed 1 dB per 10 seconds. The signal generator level should be between 0.1 and 0.5 μV.

UNLOCK SENSITIVITY (0.1-0.5 μV)_____μV

Slowly increase the signal generator level until the green LOCK light comes on. Do not exceed 1 dB per 10 seconds. The level will typically be 6 dB above the unlock level and should be between 0.25 and 1.0 μV.

LOCK LEVEL (0.25-1.0 μV)_____μV

6.3.11 Antenna Voltage Measurement

Connect the antenna to the receiver through a BNC T-connector. With the antenna connected to the receiver, measure the DC voltage at the ANTENNA input.

ANTENNA VOLTAGE (2.0V $\pm$0.2)_____V

6.3.12 Signal Strength Measurement

After the antenna has been installed and connected to the Model 8165, measure the AGC voltage. Connect the negative lead of the DVM to A2TP3 and the positive lead to A2TP6. Record the voltage. Maximize this voltage by experimenting with antenna location and orientation. The receiver will lock on the signal when the AGC voltage is greater than 1.0 volts.

AGC VOLTS (1.0 V)_____V

6.4 OSCILLATOR AND POWER SUPPLY CHECKS

These checks verify that the power supplies on the A5 assembly are operational. Refer to Figure 4-10 on page 4-19 for the component location diagram.

Connect the negative lead of a DMM to the chassis. Select the +200 VDC range and connect the positive lead to J8-3 on the rear panel. Place the rear panel selector switch in the EXT position. The DMM should read +27.6 V at 25°C ambient. This voltage will vary by -0.05 volts per degree C for room temperatures other than 25°C. If the temperature corrected voltage is not correct, adjust potentiometer A5R18 for the correct reading, and glyptol the potentiometer.

A5R18 set for +27.6 V_____

Connect the positive lead to the collector of A5Q9 (the metal side of the package). The DMM should read +21.0 volts. If it does not, adjust A5R25 for +21.0 volts.

A5Q9-C READS +21.0 V_____

6.4.1 Oscillator Alignment

Allow the oscillator to operate with uninterrupted oven and oscillator power for at least 24 hours before performing the alignment. The alignment procedure is described in Section 6.6.14, Frequency-Time Comparator Test Procedure.

6.5 ALARM TESTS

The Major and Minor Alarms are communicated by RS-422 outputs and relay contacts. A Minor Alarm is caused by an output fault or adjust oscillator alarm. A frequency, signal, or CPU alarm triggers a Major Alarm. A power failure will de-energize the major alarm relay causing a Major Alarm. Anytime a Major Alarm is activated the rear panel standard outputs will be disabled. The absence of these outputs triggers an output fault or Minor Alarm. To test the alarm outputs the receiver must be phase locked and free of any alarm conditions.

6.5.1 Minor Alarm Test

To induce a Minor Alarm place a short across one of the five rear panel standard outputs. Observe the following:

FUNCTION	LOCATION	NORMAL OPERATION	MINOR ALARM ACTIVATED
RS-422 + MINOR	AUX IN/OUT PIN 1	0.6V	2.3 V
RS-422 - MINOR	AUX IN/OUT PIN 2	2.3V	0.6 V
RELAY OUTPUTS	ALARM OUTPUTS (PINS 1 TO 2)	CLOSED	OPEN
	ALARM OUTPUTS (PINS 1 TO 3)	OPEN	CLOSED

The short must remain in place during Minor Alarm checks. The front panel output fault lamp will latch on but the Minor Alarm will clear when the short is removed.

6.5.2 Major Alarm Test

A Major Alarm may be tested by activating the signal alarm. Remove the antenna and turn the receiver off. Wait for approximately 30 seconds then turn the receiver on. The **UNLOCK SIGNAL** and **OUTPUT** lamps should be illuminated. Make the Major Alarm checks as listed below. Reconnect the antenna. Once the unit phase locks, make the checks listed in the normal operation column. The output fault lamp is turned off by depressing the RESET button.

FUNCTION	MAJOR ALARM LOCATION	NORMAL OPERATION	MAJOR ALARM ACTIVATED
RS-422 + MAJOR	AUX IN/OUT PIN 8	0.6 V	2.3 V
RS-422 - MAJOR	AUX IN/OUT PIN 9	2.3 V	0.6 V
RELAY OUTPUTS	ALARM OUTPUTS (PINS 4 TO 5)	CLOSED	OPEN
	ALARM OUTPUTS (PINS 4 TO 6)	OPEN	CLOSED

6.6 FREQUENCY-TIME COMPARATOR CHECKS

These checks verify the operation of the frequency-time comparator assembly. Before starting this section of test procedure, record the dip switch settings of U1 and U18.

The Antenna should be connected to the Model 8165. A cable should be prepared to connect the DATA terminal to J7 on the rear panel. Refer to the component location diagram, Figure 4-12 on page 4-23.

The interface at J7 DATA output is:

J7-5 Data from 8165
J7-4 Data into 8165
J7-9 Ground

The mating connector is a 9-pin series D male.

6.6.1 *Power Supplies*

Apply power to the unit and record the following voltages:

J2-6 +5 volts (±0.25) _____Volts
J2-2 +12 volts (±0.50) _____Volts
J2-1 -12 volts (±0.50) _____Volts

6.6.2 *Receiver Lock*

Set up the oscilloscope for DC coupling, auto-trigger at 1 volt/division and 10 milliseconds/division. Connect the probe ground to the chassis. The LOCK lamp on the front panel should be illuminated.

LOCK lamp illuminated _____
J4-5 RXLOCK (> +3.0 Volts) _____

Remove the antenna from the unit. Within 30 seconds the unlock lamp should illuminate.

UNLOCK lamp illuminated _____
J4-5 RXLOCK (< +0.6 Volts) _____

RECONNECT THE ANTENNA

6.6.3 *Push Button Reset*

Place the oscilloscope probe on PBRESET (J1-2).

J1-2 PBRESET (>3.0 Volts) _____

Hold front panel RESET button depressed.

J1-2 PBRESET (<0.6 Volts) _____

6.6.4 Outfault Input Test

Place oscilloscope probe on OUTFAULT (J3-5).

J3-5 OUTFAULT (>3.0 Volts) _____

Short the 10 MHz standard output on the rear panel.

J3-5 OUTFAULT (<0.6 Volts) _____

6.6.5 10 MHz Clock Inputs

Set up the oscilloscope for DC coupling, positive-trigger at 1 volt/division and 100 nanoseconds/division. Leave the probe ground on the chassis.

At NIST 10 MHz (J4-4) should be a square wave:

Period (100 ±10 nanoseconds) _____
High Level (>3.0 Volts) _____
Low Level (<0.6 Volts) _____

At STD 10 MHz (J4-1) should be a square wave:

Period (100 ±10 nanoseconds) _____
High Level (>3.0 Volts) _____
Low Level (<0.6 Volts) _____

6.6.6 Time Code Input

Change the oscilloscope timebase to 200 milliseconds per division. The oscilloscope should trigger approximately every three seconds. Place probe at TCODE (J4-6). More than one half of the waveforms observed should transition low within the first five divisions and re-transition high at 1.00 ±0.02 seconds and 2.00 ±0.02 seconds.

LOW-HIGH TRANSITION PERIOD

(1.00 ±0.02 seconds) _____
High Level (>3.0 Volts) _____
Low Level (<0.6 Volts) _____

6.6.7 Alarm Lamp Test

Turn on the LAMP and TEST switches on dip switch U1. All remaining switches on U1 and U18 should be turned off. Note that the CPU lamp flashes alternate of the FREQ, SIGNAL, OUTPUT, and ADJ OSC alarms.

LED CHECK _____

Turn off the TEST and LAMP switches and depress the reset button to clear any alarms.

6.6.8 1-Hz Output

Change the oscilloscope time base to 200 milliseconds/division. Change the trigger to positive edges. Place the probe on J7-7 on the rear panel. A 1-Hz square-wave should be observed with a high level greater than 3.0 volts and a low level less than 0.6 volts.

1-Hz OUTPUT _____

6.6.9 Signal Function Test

Remove the power from the unit. Connect the data terminal to the rear panel connector. Move U1 switches TEST and GATE to the ON position. Apply power to the unit. Initially, the UNLOCK and SIGNAL lamps will be illuminated. Within 30 seconds, the LOCK lamp should illuminate, extinguishing the UNLOCK and SIGNAL lamps.

Ten seconds after the lock lamp illuminates a frequency printout at the data terminal should begin.

6.6.10 Time Code Function Test

Within 30 seconds of the illumination of the LOCK lamp a phase printout at the computer terminal should begin.

6.6.11 GATE10 Switch Test

Move the GATE10 switch to the OFF position. One more frequency printout should occur at the end of the regular 10 second gate period. The only automatic printouts for the subsequent 1000 seconds should be phase printouts.

6.6.12 Terminal Commands

Type the letter "D" on the keyboard. "DA=500" should be printed out. Type "500" followed by a carriage return. The D/A Set Record should be printed.

Type the letter "R" on the keyboard. "Restart at" should be printed out.

Type the letter "L" on the keyboard. All records since the application of power should be reprinted.

6.6.13 D/A Switch Test

Using the DVM, measure HILIMIT (J3-4). It should read 6.5 ±0.5 volts. (Chassis ground is sufficient for the ground probe.)

Adjust LOLIMIT (J3-3), by turning R4 on the A5 board, to 3.0 ±0.3 volts.

Move the TEST and DA-ZERO switches to the ON position. Using the DVM, measure the voltage at U16-9. It should read an average of 0 ±0.2 volts.

Move the DA-ZERO switch to the OFF position and move the DA-ONE switch to the ON position. The voltage at U15-6 should change to 3.5 ±0.5 volts.

6.6.14 Frequency Range Adjustment

Before performing the oscillator alignment the unit must be connected to an uninterrupted power source a minimum of 24 hours in advance.

The antenna must be connected and the receiver must be phase locked.

Move the TEST, GATE10, and DA-ZERO switch to the ON position. Type "R" on the data terminal. Approximately every ten seconds, a frequency record will be printed. The frequency printouts are in hexidecimal. Adjust the coarse frequency trim on the ovenized oscillator until three consecutive frequency printouts of 000005F5E119 ±1 are achieved. (Counter-clockwise rotation of the trimmer will increase frequency.)

000005F5E119 ±1 _____

Units equipped with Option 31, 10-Hz TV Offset only, set oscillator to:

000005F5E123 ±1 _____

Move the DA-ZERO switch to the OFF position and move the DA-ONE switch to the ON position. Similarly, adjust R4 on the A5 board until three consecutive printouts of 000005F5E0B5 ±2 are achieved. (Counter-clockwise rotation will increase frequency.)

000005F5E0B5 ±2 _____

Option 31 Units only:

000005F5EBF ±2 _____

The receiver alignment and performance tests are now complete. Return DIP switches U12 and U18 to their original positions. The unit will require a 3 to 4 hour re-synchronization period. Once the frequency alarm lamp has extinguished the output fault lamp may be turned off by depressing the reset button. The unit may now be returned to service.

6.7 ACCESSORY TESTS

This section provides information on testing the following:

* Model 8206A Antenna
* Model 8207 Preamp
* Model 8140T Line Tap

6.7.1 Model 8206A Antenna

This test verifies the proper operation of the Model 8206A Loop Antenna.

Figure 6-2, MODEL 8206A TEST SET-UP shows the test set-up for testing the antenna. Connect a coax cable to the signal generator. Wrap 2 turns of wire around the antenna. Connect one side of the wire to the center conductor of the coax through a 1K resistor. Connect the other side to the shield.

Adjust the signal generator for an output of .014 V rms into the 1K load. If the signal generator has a calibrated output that expects a 50-ohm load, then adjust the output level to .007 V rms. Feed +12V to the antenna through a 27K resistor. AC couple the antenna to the scope.

Find the resonant frequency of the antenna by adjusting the signal generator frequency for maximum output signal. The resonant frequency should be 60.0 ± .3 kHz.

RESONANT FREQUENCY 60.0 ±.3 kHZ_____kHZ

The amplitude of the output signal should be approximately 0.01 Vp-p.

ANTENNA OUTPUT (.010 Vp-p) _____V

Determine the antenna bandwidth. Increase the signal generator frequency until the output amplitude is 3 dB below the resonant frequency amplitude. Decrease the signal generator frequency until the output amplitude is 3 dB down. Make sure that the amplitude of the input signal remains constant during this test. The antenna bandwidth is the difference in the two frequencies.

ANTENNA BANDWIDTH (1 kHz)_____kHz

WARNING: ALL OTHER ANTENNAS EXCEPT UNIT UNDER TEST MUST BE KEPT AT LEAST 6 FEET AWAY TO PREVENT STRAY DETUNING! DO NOT PLACE ANTENNA ON OR NEAR METAL SURFACES OR OBJECTS.

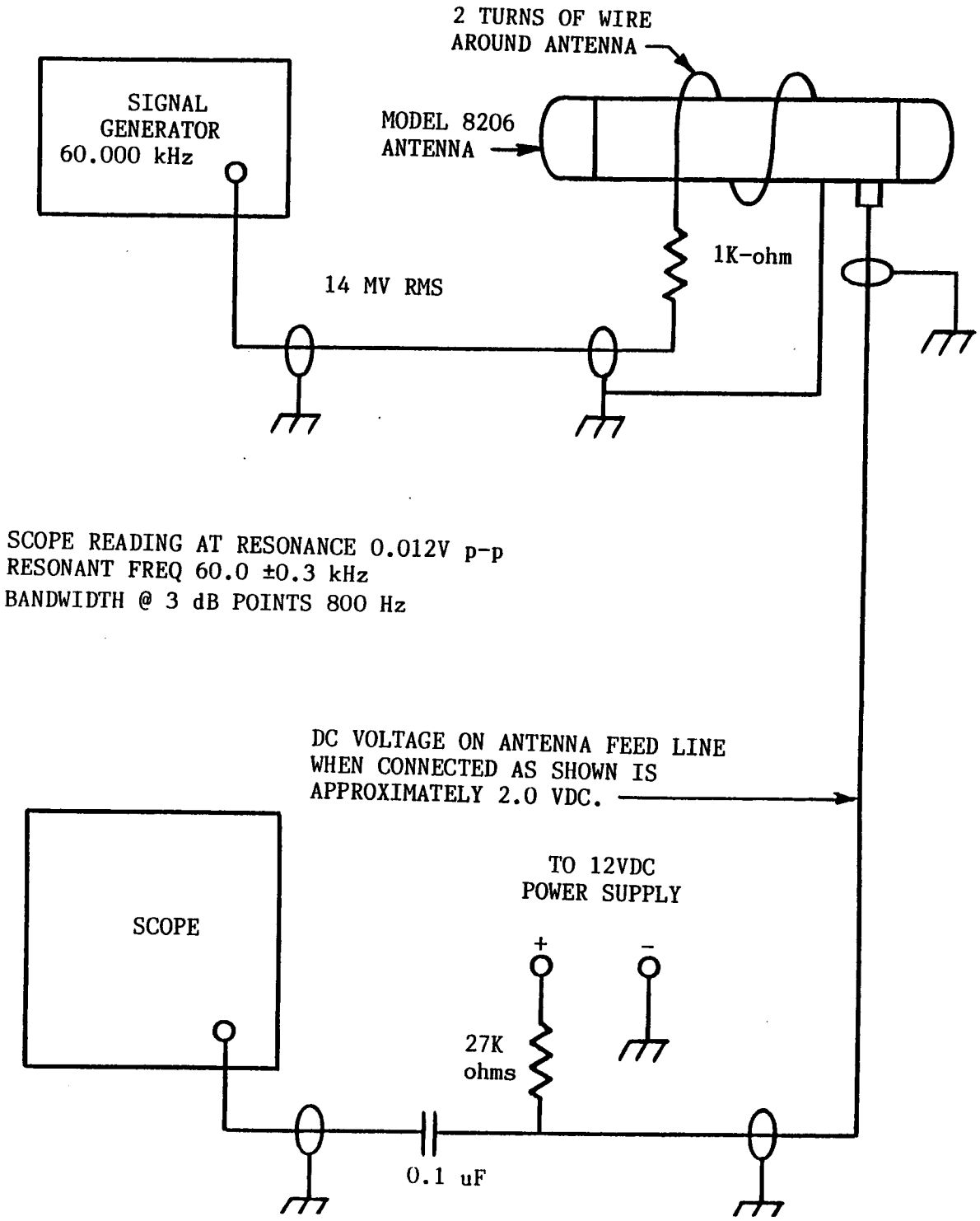


FIGURE 6-2 ANTENNA MODEL 8206A TEST SET-UP

6.7.2 Model 8207 Preamp Alignment

The Model 8207 Antenna Preamplifier is a low noise, tuned, 60 kHz line amplifier used in the antenna feed line wherever the WWVB signal strength is less than 0.3 μV at the receiver antenna terminator.

The purpose of this test is to tune the preamp to 60 kHz.

Perform the receiver alignment as described in this section.

Set the receiver A1S1 switch to the preamp (P) position.

Use RG-58 coax to connect the preamp between the signal generator and the WWVB receiver as shown in Figure 6-3.

Physically separate the preamp from the receiver by at least 10 feet. Keep the cable from the signal generator to the preamp away from the vicinity of the receiver to prevent signal regeneration.

In the receiver, disconnect the AGC wire (violet) from connector A1P2, Pin 6, but leave the remaining wires in place and the connector mated.

Connect an oscilloscope probe to A1E3. Set the scope for AC coupling. The ground lead is connected to the chassis.

Set the generator to provide a 1.0 μV signal at exactly 60.000 Hz, unmodulated.

Apply power to the receiver and adjust the signal generator level as necessary to provide a 1 Vp-p output signal on the oscilloscope.

Adjust the slug in transformer A1T1 in the Model 8207 for a peak on the oscilloscope, while reducing the signal generator level to maintain the 1 Vp-p output.

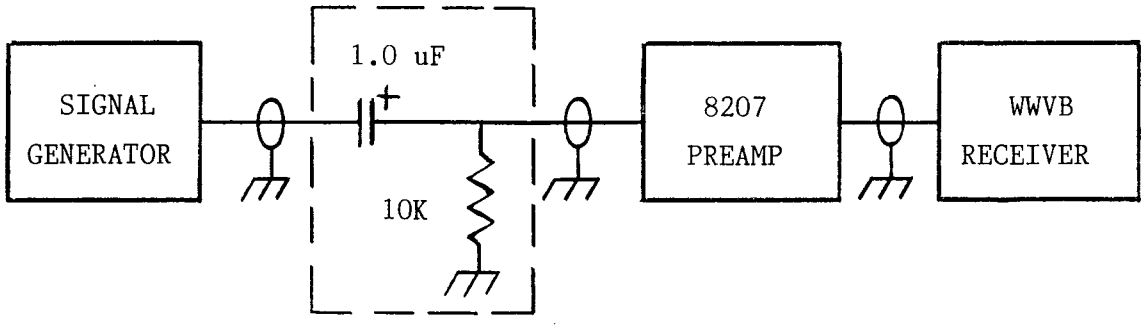


FIGURE 6-3 MODEL 8207 PREAMPLIFIER ALIGNMENT

6.7.3 Model 8140T Line Tap Test Procedure

Refer to Figure 6-4 Line Tap Model 8140T Test Setup. Connect a coaxial BNC tee to the output of the line tap under test. Connect the 50-ohm load to one output of the tee and connect the oscilloscope to the other tee output.

Set the scope for DC coupling and set the sweep at 1 cycle/cm.

The oscilloscope presentation should be a 1.4 Vp-p minimum. (2.0 Vp-p typical) sine wave symmetrical around the 0 volt reference.

Remove the 50-ohm output termination. The scope should show 3.0 Vp-p minimum (4.0 Vp-p typical) sine wave with a DC offset as shown.

NOTE: At frequencies of 5 or 10 MHz, a 10:1 oscilloscope probe must be used to prevent loading.

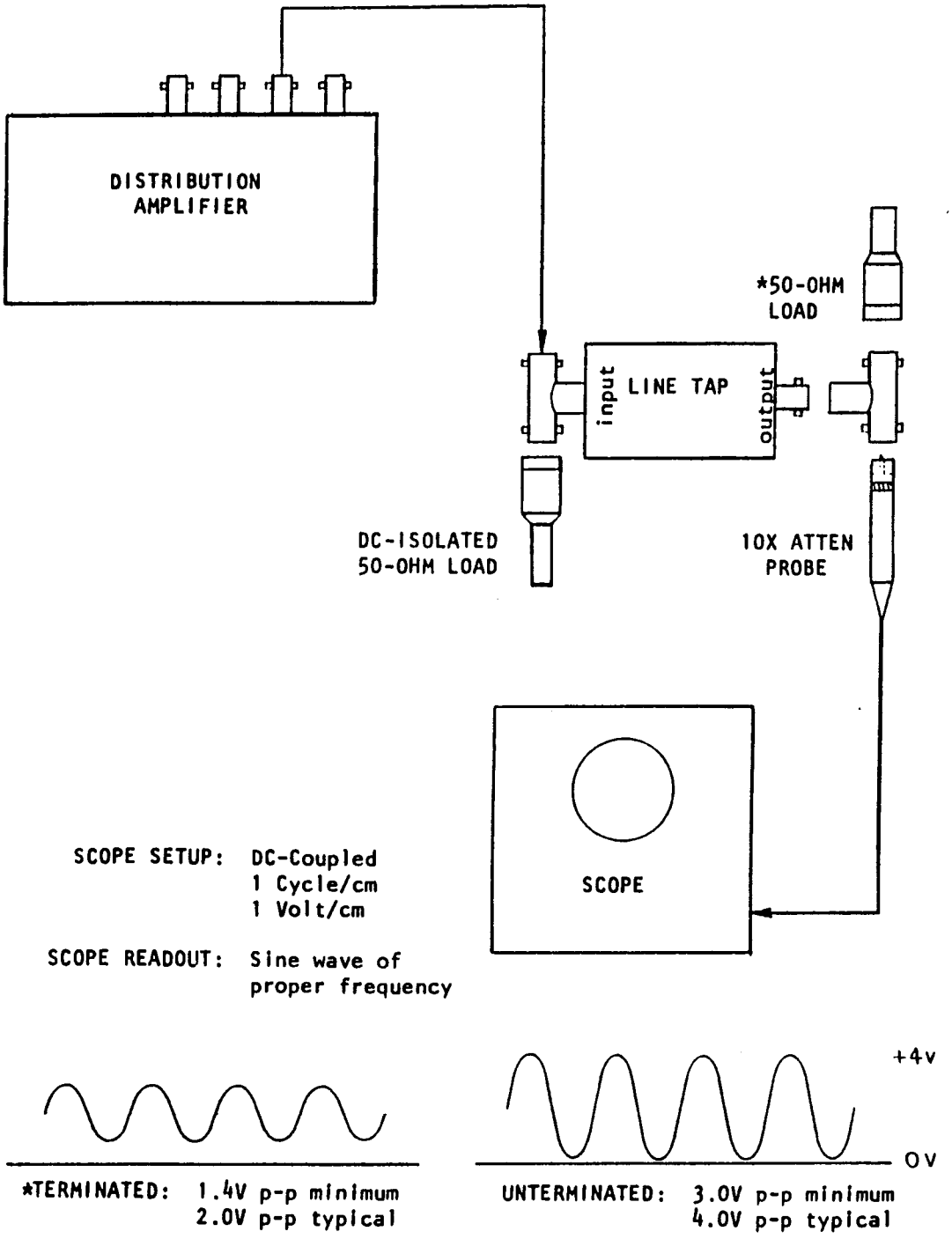


FIGURE 6-4 LINE TAP MODEL 8140T TEST SET-UP

6.8 OFFSET PERFORMANCE TEST

This section provides a method on testing the Model 8165 frequency offsets.

6.8.1 Equipment Needed

*Spectracom Model 8150, Precision Phase Comparator
*Spectracom Model 8212 Strip Chart Recorder (Optional)
*Tektronix TM500/5000 Mainframe
*10-MHz standard with accuracy better than $1x10^{-10}$
*Stopwatch

6.8.2 Test Set-Up

Prior to performing the following test, the Model 8165 must be phase-locked to WWVB and in continuous operation for at least 24 hours.

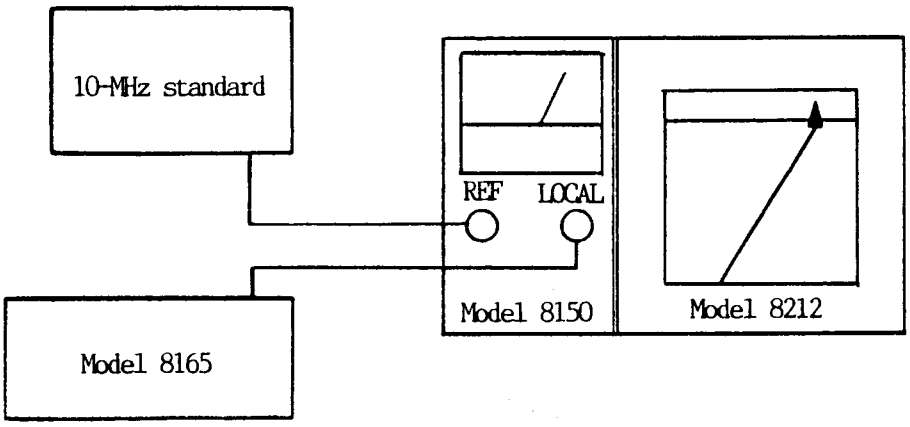


FIGURE 6-5 OFFSET TEST SET-UP

- Connect the 10-MHz standard to the reference input connector of the Model 8150.
- Connect the Model 8165 to the Model 8150 local input connector.
- The Model 8212, Strip Chart Recorder provides a permanent record of the phase comparison. The chart recorder allows practical long-term observations over hours or days, thus increasing the potential resolution of the measurement.

6.8.3 Procedure

The Model 8150 panel meter displays the phase drift between the two signals. The panel meter scale is in microseconds of relative time. The scale factor is determined by the "N" factor button depressed and the input frequency. The following tables list the various offsets available and the time for a full scale deflection for a given "N" factor. To test an offset refer to the corresponding table and set the Model 8150 to the given switch setting. With a stopwatch, measure the time it takes the meter needle to move from end to end of the scale. The needle will move from left to right with positive offsets and right to left with negative offsets. As the needle reaches one end of the scale it will return to the opposite end of the scale and begin again its travel in the same direction. It is at this switch over point that the stopwatch should be started and stopped. Compare the time measured with the stopwatch against the time listed in the table.

STANDARD SIMULCAST OFFSETS

Offset Step	Switch Settings A6U18-2,3,4,5	Fractional Frequency Offset X($1x10^{-9}$)	8150 Switch Setting	Time For End to End Meter Deflection
1	0001	6.6	N = 10	2 Min 32 Sec
2	0010	13.2	N = 100	12 Min 38 Sec
3	0011	19.2	N = 100	8 Min 41 Sec
4	0100	26.5	N = 100	6 Min 17 Sec
5	0101	33.1	N = 100	5 Min 2 Sec
6	0110	39.7	N = 100	4 Min 12 Sec
7	0111	46.4	N = 100	3 Min 36 Sec
8	1000	53.0	N = 100	3 Min 9 Sec
9	1001	59.6	N = 100	2 Min 48 Sec
10	1010	66.2	N = 100	2 Min 31 Sec
11	1011	72.8	N = 100	2 Min 17 Sec
12	1100	79.5	N = 100	2 Min 6 Sec
13	1101	86.1	N = 100	1 Min 56 Sec
14	1110	92.7	N = 100	1 Min 48 Sec
15	1111	99.3	N = 100	1 Min 41 Sec

TABLE 6-2 STANDARD SIMULCAST OFFSETS

OPTION 31, TEN HERTZ CHANNEL OFFSETS

Channel Selected	Switch Settings A6U18-2,3,4,5	Fractional Frequency Offset X($1x10^{-9}$)	8150 Switch Setting	Time for End to End Meter Deflection
2	0010	181.0	N = 1000	9 Min 12 Sec
3	0011	163.2	N = 1000	10 Min 13 Sec
4	0100	148.7	N = 1000	11 Min 12 Sec
5	0101	129.4	N = 1000	12 Min 53 Sec
6	0110	120.1	N = 1000	13 Min 53 Sec
7	0111	57.1	N = 100	2 Min 55 Sec
8	1000	55.2	N = 100	3 Min 1 Sec
9	1001	53.4	N = 100	3 Min 7 Sec
10	1010	51.7	N = 100	3 Min 13 Sec
11	1011	50.2	N = 100	3 Min 19 Sec
12	1100	48.7	N = 100	3 Min 25 Sec
13	1101	47.3	N = 100	3 Min 31 Sec

TABLE 6-3 OPTION 31, TEN-HERTZ CHANNEL OFFSETS

OPTION 56, OPTIONAL SIMULCAST OFFSETS

Offset Step	Switch Settings A6U18-2,3,4,5	Fractional Frequency Offset X($1X10^{-9}$)	8150 Switch Setting	Time for End to End Meter Deflection
1	0001	1.1	N = 10	15 Min 9 Sec
2	0010	2.2	N = 10	7 Min 35 Sec
3	0011	3.3	N = 10	5 Min 3 Sec
4	0100	4.4	N = 10	3 Min 47 Sec
5	0101	5.5	N = 10	3 Min 2 Sec
6	0110	6.6	N = 10	2 Min 32 Sec
7	0111	7.7	N = 10	2 Min 10 Sec
8	1000	8.8	N = 10	1 Min 54 Sec
9	1001	9.9	N = 10	1 Min 41 Sec
10	1010	11.1	N = 100	15 Min 1 Sec
11	1011	12.2	N = 100	13 Min 40 Sec
12	1100	13.3	N = 100	12 Min 32 Sec
13	1101	14.4	N = 100	11 Min 34 Sec
14	1110	15.5	N = 100	10 Min 45 Sec
15	1111	16.6	N = 100	10 Min 2 Sec

TABLE 6-4 OPTION 56, OPTIONAL PAGING OFFSETS

6.8.4 *Special Considerations when Using the Model 8212 Chart Recorder*

The chart speed of the Model 8212 is factory set at 20 mm/hour. This is the recommended chart speed when recording offsets less than 30×10^{-9}. Recording offsets greater than 30×10^{-9} requires changing the chart speed cam to 60 mm/hour. The faster chart speed improves the measurement resolution at the higher offsets. The 60 mm/hour cam may be found in the Model 8212 ancillary kit and is installed per instructions outlined in the chart recorder manual.

The Model 8150 should be set to the least sensitive scale, N=1000, for all offsets. This setting will produce usable chart recordings of the resultant phase comparison. Refer to the Model 8150 instruction manual for information on interpreting chart recordings.

6.9 *TROUBLESHOOTING*

If trouble occurs with a WWVB receiver, some simple checks can isolate the problem to specific areas of the receiver. Some of the more likely problems and the procedures for solving them are as follows:

1. Receiver does not lock - Improper reception. The most efficient way of solving this type of problem is to isolate the problem to one of the three major receiver system components. These are antenna, A1 RF amplifier assembly, and A2 receiver board assembly.

   A. Antenna DC check. Measure the DC voltage on the antenna line with a DVM. With the antenna connected to the receiver and the receiver turned on, the DC voltage on the coaxial line should be approximately 2.0 volts $\pm 10\%$. This can be measured by inserting a coaxial tee in the line at the rear of the receiver and measuring the antenna voltage with the antenna connected. With the antenna disconnected the DC voltage at the antenna terminal of the receiver should be approximately 11.5 volts DC $\pm 10\%$. If both these measurements are satisfactory, proper DC conditions are verified in both the antenna and its power supply in the receiver.

   If the 11.5 volt level is not present with the antenna disconnected, the fault is in either the A1 RF Amplifier assembly or in the A2 Receiver assembly. Disconnect the A1 board and check for +12 VDC at Pin 1 of the connector A1P2. If the voltage is not present, the problem is in the power supply on the A2 board assembly (diodes CR12 through CR14, capacitors C53 through C57, or regulator U22.) If the 12 volt level is present, the problem is in the A1 board assembly.

   B. Check the receiver without the antenna connected. Using a signal generator set at 60.000 kHz with an accuracy of $\pm 1 \times 10^{-6}$, feed a 1.0 microvolt signal from the generator to the antenna input of the receiver.

Apply power to the receiver and see if the receiver locks. If it does lock under this condition, the problem is most likely with the RF performance of the antenna or with the antenna placement or installation. If the receiver does not lock with 1.0 microvolts applied, the fault is in the receiver.

Check the 60 kHz signal at E3 of RF amplifier board A1. If the signal is present, the RF amplifier is operating satisfactorily and the problem is in Receiver assembly board A2. If the 60 kHz signal is not present at E3, the fault is in the A1 board assembly.

2. No NIST Output at the AUX IN/OUT connector - Check Pin 11 of U5A on the A2 board to see that the oscillator stage containing A2Y1 is operating properly, and oscillating at 10.0 MHz. If this oscillator, which gets phase locked to WWVB, is not oscillating then the most likely problem is with the crystal Y1, which may need to be replaced. Another possibility is oscillator alignment. If this oscillator stage is not performing properly, the NIST output will not be present, and the receiver will not phase lock, or alternatively the phase lock lamp may remain on continuously even though the receiver is not operating properly. This condition can be checked by removing the antenna signal and checking to see that the phase lock lamp is extinguished after approximately 30 seconds.

3. No standard output - If the front panel output from the internal frequency standard oscillator is not present, the fault can lie with either assemblies A4 or A5. The A5 oscillator assembly is the source of this signal and contains both the oscillator and its power supply. If any of these are malfunctioning the frequency standard outputs will be missing. Assembly A4 is the output amplifier which feeds the appropriate frequencies from the A5 assembly to both the front and rear panels. Signal tracing from the input of this board to the outputs which feed the front and rear panels can establish whether or not this board is performing properly.

4. Fuse blows - This problem is most likely caused by power supply malfunction in the A2 board or in the chassis power supply components such as power transformers, filter capacitors, etc. The problem may be isolated to on or off-board causes by disconnecting all of the connectors from the A2 board and turning the unit on again. If the fuse still blows the cause is not on the A2 board. If the fuse does not blow with the connectors removed from the A2 board, reconnect them in the following order, turning power on after each connector is reattached:

   A. Reattach the connector from the cable harness to A2J2. This connects the power transformers to the power supply rectifier circuits. If this causes the fuse to blow, the problem is most likely a power supply short on the A2 board itself. Check the voltage regulators U21, U22, and U23 for proper operation. Check to see that Zener diode VR2 is not shorted to ground. This diode provides over-voltage protection on the +5 VDC line and will fuse, shorting to ground causing a fuse to blow if U21 fails and lets the +5 volts go high. Before replacing VR2,

disconnect it and check U21 for proper operation. If connecting the cable at A2J2 does not cause the fuse to blow after power is reapplied, proceed to the next step.

B. Connect the A1 assembly to A2J5. Reapply power.

C. Connect the cable harness connector to A2J1. Reapply power. If this causes the fuse to blow, the problem is most likely in the A4 or A5 assemblies, perhaps a power supply short circuit on one of these boards.

D. Reconnect the cables at A2J3 and A2J4. A2J3 provides +5 volts DC to the other parts of the receiver, including the front panel and a short on one of these lines will cause a fuse to blow.

5. Output fault light on - The output fault lamp indicates that a rear panel output is not present. First check to see that the unit is not exhibiting a Major Alarm. A Major Alarm will disable the rear panel outputs. Otherwise, check that the outputs are not being loaded down by a device using the standard outputs. Impedance mismatch can cause reflections which will cancel the signal. Terminate the end of any coaxial line with a 50 ohm load to prevent reflections.

6. TERMINAL COMMANDS

If there is no response to letters typed at the terminal, repeatedly type characters and look for ASCII data at U27-1 and U13-10. If data is present, suspect the processor chip.

If the "L" command does not produce a replication of the previous records, suspect the RAM chip, U5.

7. D/A SWITCH TEST

If HILIMIT does not have 6.5 volts, check A5, Oscillator Assembly.

If LOLIMIT cannot be adjusted to 3.0 volts, check A5, Oscillator Assembly.

If the DA-ZERO switch does not produce zero volts at U15-6, verify that the DA-ZERO switch is operative by checking for a low at U7-39 when the switch is ON and a high when the switch is OFF. Also verify that the DA-ONE switch is not defective by checking for a high at U7-38. If the switches check out, then the PPI (U7), the D/A unit (U16), or the Op Amp (U15) may be at fault.

If the DA-ONE switch does not produce the expected results, verify that the switch is operative by checking for a low at U7- 38 when the switch is ON and a high when the switch is OFF. Also check the DA-ZERO switch at U7-39. If the switches check out, measure the voltage at U16-8, it should be approximately -3.5 volts. If not, check the preceding differential amplifier. If U16-8 was satisfactory, then the PPI (U7), the D/A unit (U16), or the OpAmp (U15) may be at fault.

8. FREQUENCY RANGE ADJUSTMENT

If 000005F5E119 coarse adjustment cannot be achieved, check U19-14 for approximately 6.5 $\pm$0.3 volts. If this voltage is not present, check the associated differential amplifier.

If difficulty is encountered in adjusting R4 on the A5 board for 000005F5EOB5, measure the voltage at J3-3. U19-14 should be equal to that voltage $\pm$0.5 volts. If not, check the associated differential amplifier.

9. PROCESSOR CHECK

The central control element of the FTC is a microprocessor subsystem including a microprocessor, a read-only memory (ROM), and a random-access memory (RAM). To provide for the FTC functions, the processor utilizes a variety of hardware devices including counter/timers and basic input/output lines.

The rational behavior of the FTC relative to these various input/output sources is determined by instructions stored in the ROM.

The inner workings of the processor subsystem are rather complex, so the following procedures have been constructed to aid in troubleshooting the processor subsystem.

Remove the power from the unit. Move all switches on U1 and U18 to the OFF position. Move the PHASE, FREQ, TEST, and GATE10 switches to the ON position. Apply power to the unit. Verify the following measurements after LOCK condition:

Logic level	50 kHz waveform at U3-10	_____
Logic level	1 Hz waveform at U3-13	_____
Logic level	50 kHz waveform at U2-10	_____
Logic level	1 Hz waveform at U2-13	_____
Logic level	200 Hz waveform at U2-17	_____

If the above conditions exist, the internals of (CPU) U13, U12, U2, and U3 are probably good.

If none of the above are functional, check U13-18 for a low level 11 MHz signal. This verifies the CPU oscillator circuit and crystal. Check for a high going pulse at U12-11 every 1 to 2 microseconds for approximately 100 nanoseconds. Check for a low going signal of 200 nanoseconds at U6-20. This verifies the CPU instruction fetch cycle. Connect the oscilloscope to U5-21. Set for negative triggering with a sweep of 2 microseconds/division. Momentarily turn the power off and back on again. Pulses should appear here every 3 to 6 microseconds for more than 100 milliseconds. If so, U6 and U12 are probably good. U8 is probably faulty.

If U2 readings above are good but the U3 readings are not, check for a 200+ nanosecond low going pulse at U8-14 at least 10 times per second. If it is present, U3 is probably faulty, otherwise U8 is probably faulty.

If U3 readings above are good but the U2 readings are not, check for 200+ nanosecond low going pulses at U8-13 at least 10 times per second. If present, U2 is probably faulty, otherwise U8 is probably faulty.

Check for 200+ nanosecond low-going pulses at U8-12 at least 10 times per second. If they are not present, U8 is probably faulty.

If switches or lamps do not behave normally at this point, U7 is probably faulty.

MODEL 8165

SECTION 7

PARTS LIST

REPLACEABLE PARTS

The parts lists on the following pages include mainframe components, circuit board assemblies and PC board components that are replaceable. Refer to the schematic diagrams to determine which optional parts are used in the equipment you have. To order a complete PC board assembly, list the PC board assembly number followed by the appropriate option numbers.

REPLACEABLE PARTS - 8165 MAINFRAME

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
C001	C26474	CAP, 0.47 μF, 50V DISC CERAMIC
C002	C26474	CAP, 0.47 μF, 50V DISC CERAMIC
C003	C00300	CAP, 8900 μF 25V ELEC.
DS01	DS00042	LED, RED
DS02	DS00045	LED, GREEN
DS03	DS00042	LED, RED
DS04	DS00042	LED, RED
DS05	DS00042	LED, RED
DS06	DS00042	LED, RED
DS07	DS00042	LED, RED
F001	F00R75	FUSE, 3/4A, 3AG
F001	F001R2	FUSE, 1-1/4A, 3AG, OPT 03
F002	F001R0	FUSE, 1.0A, 3AG Opt 55
F002	F00R38	FUSE, 3/8A, 3AG
J001	J00010	RECEPTACLE, BNC SHORT SHANK
J002	J00010	RECEPTACLE, BNC SHORT SHANK
J003	J00010	RECEPTACLE, BNC SHORT SHANK
J004	J00010	RECEPTACLE, BNC SHORT SHANK
J005	J00010	RECEPTACLE, BNC SHORT SHANK
J009	J00002	RECEPTACLE, BNC
J010	J01005	JACK, FILTER/POWER
J011	J00010	RECEPTACLE, BNC SHORT SHANK
LUG1	H00040	SOLDER LUG #4
S001	S00221	SWITCH, SPDT LOCKING LEVER
S002	S00102	SWITCH, DPDT SLIDE
S003	S00421	SWITCH, MOMENTARY PB
T001	T10000	TRANSFORMER, MAIN PWR SUPPLY
T002	T10001	TRANSFORMER, OSC SUPPLY
TB01	TB00300	TERMINAL BLOCK, 2 POS (DC INPUT OPTIONS ONLY)
XF01	X00049	FUSEHOLDER
XF02	X00049	FUSEHOLDER

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
A1	001100	PC BOARD ASSEMBLY, RF AMPLIFIER
C001	C07220	CAP, 22 μF 25V LITIC
C002	C06182	CAP, 1800pF MICA
C003	C09010	CAP, 1.0 μF 50V LITIC
C004	C09010	CAP, 1.0 μF 50V LITIC
C005	C09010	CAP, 1.0 μF 50V LITIC
C006	C07220	CAP, 22 μF 25V LITIC
C007	C05820	CAP, 82pF MICA
C008	C00040	CAP, 4.5-20 pF CER. TRIM
C009	C00040	CAP, 4.5-20 pF CER. TRIM
C010	C05050	CAP, 5pF MICA
C011	C09010	CAP, 1.0 μF 50V LITIC
C012	C07220	CAP, 22 μF 25V LITIC
C013	C09010	CAP, 1.0 μF 50V LITIC
C014	C18103	CAP, 10000 pF 65V POLYSTYRENE
C015	C18103	CAP, 10000 pF 65V POLYSTYRENE
C016	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C017	C09010	CAP, 1.0 μF 50V LITIC
C018	C07220	CAP, 22 μF 25V LITIC
C019	C09010	CAP, 1.0 μF 50V LITIC
C020	C09010	CAP, 1.0 μF 50V LITIC
C021	C09010	CAP, 1.0 μF 50V LITIC
C022	C07220	CAP, 22 μF 25V LITIC
C023	C06182	CAP, 1800pF MICA
L001	L03102	CHOKE, 1000 UH
L002	L03102	CHOKE, 1000 UH
L003	L03331	CHOKE, 330 UH
P001	J00002	RECEPTACLE, BNC
P002	P04014	PLUG, 6 PIN
P02E	P00300	KEY, MOLEX
Q001	Q04126	TRANSISTOR, PNP, 2N4126
Q002	Q04124	TRANSISTOR, NPN, 2N4124
Q003	Q04124	TRANSISTOR, NPN, 2N4124
R001	R01562	RES, 5.6K OHMS 1/4W 5% C.FILM
R002	R01273	RES, 27K OHMS 1/4W 5% C.FILM
R003	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R004	R01183	RES, 18K OHMS 1/4W 5% C.FILM
R005	R01153	RES, 15K OHMS 1/4W 5% C.FILM
R006	R01152	RES, 1.5K OHMS 1/4W 5% C.FILM
R007	R01123	RES, 12K OHMS 1/4W 5% C.FILM
R008	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R009	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R010	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R011	R01183	RES, 18K OHMS 1/4W 5% C.FILM
R012	R01183	RES, 18K OHMS 1/4W 5% C.FILM
R013	R01123	RES, 12K OHMS 1/4W 5% C.FILM

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
R014	R01683	RES, 68 K OHMS 1/4W 5% C.FILM
R015	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R016	R01681	RES, 680 OHMS 1/4W 5% C.FILM
R017	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R018	R01100	RES, 10 OHMS 1/4W 5% C.FILM
R019	R05503	POT, 50K OHM TRIM
R020	R01222	RES, 2.2K OHMS 1/4W 5% C.FILM
S001	S00420	SWITCH, SLIDE
T001	T00020	TRANSFORMER, INPUT
U001	U01350	IF AMP, 1350
U002	U01350	IF AMP, 1350
Y001	Y00000	XTAL, 60 KHZ
A2	001200	PC BOARD ASSEMBLY, RECEIVER
C001	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C002	C09010	CAP, 1.0 μF 50V LITIC
C003	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C004	C00100	CAP, 120 μF 15V TANT.
C005	C02103	CAP, .01 μF 25V DISC CERAMIC
C006	C07220	CAP, 22 μF 25V LITIC
C007	C15685	CAP, 6.8 μF 35V TANT
C008	C05560	CAP, 56pF MICA
C009	C05200	CAP, 20pF MICA
C010	C00040	CAP, 4.5-20 pF CER. TRIM
C011	C05121	CAP, 120pF MICA
C012	C05301	CAP, 300pF MICA
C013	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C014	C18472	CAP, 4700 pF 65V POLYSTYRENE
C015	C18472	CAP, 4700 pF 65V POLYSTYRENE
C016	C09010	CAP, 1.0 μF 50V LITIC
C017	C07220	CAP, 22 μF 25V LITIC
C018	C07220	CAP, 22 μF 25V LITIC
C019	C09010	CAP, 1.0 μF 50V LITIC
C020	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C021	C15105	CAP, 1 μF 35V TANT
C022	C10157	CAP, 150 μF 6V TANT
C023	C07220	CAP, 22 μF 25V LITIC
C024	C02103	CAP, .01 μF 25V DISC CERAMIC
C025	C02103	CAP, .01 μF 25V DISC CERAMIC
C026	C02103	CAP, .01 μF 25V DISC CERAMIC
C027	C02103	CAP, .01 μF 25V DISC CERAMIC
C028	C02103	CAP, .01 μF 25V DISC CERAMIC
C029	C02103	CAP, .01 μF 25V DISC CERAMIC
C030	C02103	CAP, .01 μF 25V DISC CERAMIC
C031	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C032	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C033	C01104	CAP, 0.1 μF 25V DISC CERAMIC

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
C034	C07220	CAP, 22 μF 25V LITIC
C035	C07220	CAP, 22 μF 25V LITIC
C036	C02103	CAP, .01 μF 25V DISC CERAMIC
C037	C02103	CAP, .01 μF 25V DISC CERAMIC
C038	C02103	CAP, .01 μF 25V DISC CERAMIC
C039	C05910	CAP, 91pF MICA
C040	C05910	CAP, 91pF MICA
C041	C02103	CAP, .01 μF 25V DISC CERAMIC
C042	C02103	CAP, .01 μF 25V DISC CERAMIC
C043	C02103	CAP, .01 μF 25V DISC CERAMIC
C044	C18392	CAP, 3900 pF 65V POLYSTYRENE
C045	C18751	CAP, 750 pF 65V POLYSTYRENE
C046	C18392	CAP, 3900 pF 65V POLYSTYRENE
C047	C07222	CAP, 2200 μF 25V LITIC
C048	C07222	CAP, 2200 μF 25V LITIC
C049	C07222	CAP, 2200 μF 25V LITIC
C050	C07222	CAP, 2200 μF 25V LITIC
C051	C09010	CAP, 1.0 μF 50V LITIC
C052	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C053	C08102	CAP, 1000 μF 35V LITIC
C054	C08102	CAP, 1000 μF 35V LITIC
C055	C09010	CAP, 1.0 μF 50V LITIC
C056	C09010	CAP, 1.0 μF 50V LITIC
C057	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C058	C01104	CAP, 0.1 μF 25V DISC CERAMIC
C059	C09010	CAP, 1.0 μF 50V LITIC
C060	C09010	CAP, 1.0 μF 50V LITIC
CR01	CR04148	DIODE, IN4148
CR02	CR00209	VARICAP,29 pF,3V
CR03	CR05059	RECTIFIER,1A,200 PIV
CR04	CR04148	DIODE, IN4148
CR06	CR04148	DIODE, IN4148
CR07	CR04148	DIODE, IN4148
CR08	CR05624	RECTIFIER,3A,200 PIV
CR09	CR05624	RECTIFIER,3A,200 PIV
CR10	CR05624	RECTIFIER,3A,200 PIV
CR11	CR05624	RECTIFIER,3A,200 PIV
CR12	CR05059	RECTIFIER,1A,200 PIV
CR13	CR05059	RECTIFIER,1A,200 PIV
CR14	CR05059	RECTIFIER,1A,200 PIV
CR15	CR05059	RECTIFIER,1A,200 PIV
CR16	CR04148	DIODE, IN4148
J001	J10014	HEADER, 6 PIN (4)
J002	J10014	HEADER, 6 PIN (2)
J003	J10014	HEADER, 6 PIN (2)
J004	J10014	HEADER, 6 PIN (2)
J005	J10014	HEADER, 6 PIN
L001	L03152	CHOKE, 1500 UH
L002	L03152	CHOKE, 1500 UH

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
L003	L03152	CHOKE, 1500 UH
Q001	Q04126	TRANSISTOR, PNP, 2N4126
Q002	Q04126	TRANSISTOR, PNP, 2N4126
Q003	Q04124	TRANSISTOR, NPN, 2N4124
Q004	Q04258	TRANSISTOR, PNP, PN 4258-18
Q005	Q04126	TRANSISTOR, PNP, 2N4126
Q006	Q04258	TRANSISTOR, PNP, PN 4258-18
Q007	Q04258	TRANSISTOR, PNP, PN 4258-18
Q008	Q04126	TRANSISTOR, PNP, 2N4126
Q009	Q04124	TRANSISTOR, NPN, 2N4124
R001	R01471	RES, 470 OHMS 1/4W 5% C.FILM
R002	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R003	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R004	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R005	R05202	POT, 2K OHM TRIM
R006	R21512	RES, 5.1K OHMS 1/4W 2% M.FILM
R007	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R008	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R009	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R010	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R011	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R012	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R013	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R014	R05502	POT, 5K OHM TRIM
R015	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R016	R01562	RES, 5.6K OHMS 1/4W 5% C.FILM
R017	R01562	RES, 5.6K OHMS 1/4W 5% C.FILM
R018	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R019	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R020	R01153	RES, 15K OHMS 1/4W 5% C.FILM
R021	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R022	R01330	RES, 33K OHMS 1/4W 5% C.FILM
R023	R05102	POT, 1K OHM TRIM
R024	R01331	RES, 33 OHMS 1/4W 5% C.FILM
R025	R01471	RES, 470 OHMS 1/4W 5% C.FILM
R026	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R027	R01561	RES, 560 OHMS 1/4W 5% C.FILM
R028	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R029	R01152	RES, 1.5K OHMS 1/4W 5% C.FILM
R030	R05202	POT, 2K OHM TRIM
R031	R21512	RES, 5.1K OHMS 1/4W 2% M.FILM
R032	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R033	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R034	R01473	RES, 47K OHMS 1/4W 5% C.FILM
R035	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R036	R01153	RES, 15K OHMS 1/4W 5% C.FILM
R037	R01153	RES, 15K OHMS 1/4W 5% C.FILM
R038	R21154	RES, 150K OHMS 1/4W 2% M.FILM
R039	R21153	RES, 15K OHMS 1/4W 2% M.FILM

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
R040	R21154	RES, 150K OHMS 1/4W 2% M.FILM
R041	R01122	RES, 1.2K OHMS 1/4W 5% C.FILM
R042	R01153	RES, 15K OHMS 1/4W 5% C.FILM
R043	R01475	RES, 4.7M OHMS 1/4W 5% C.FILM
R044	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R045	R01473	RES, 47K OHMS 1/4W 5% C.FILM
R046	R01563	RES, 56K OHMS 1/4W 5% C.FILM
R047	R01394	RES, 390K OHMS 1/4W 5% C.FILM
R048	R01105	RES, 1 M OHMS 1/4W 5% C.FILM
R049	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R050	R01221	RES, 220 OHMS 1/4W 5% C.FILM
R051	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R052	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R053	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R054	R01332	RES, 3.3K OHMS 1/4W 5% C.FILM
R055	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R056	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R057	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R058	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R059	R01682	RES, 6.8K OHMS 1/4W 5% C.FILM
R060	R01471	RES, 470 OHMS 1/4W 5% C.FILM
R061	R01471	RES, 470 OHMS 1/4W 5% C.FILM
R062	R01391	RES, 390 OHMS 1/4W 5% C.FILM
R063	R01152	RES, 1.5K OHMS 1/4W 5% C.FILM
R065	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R066	R01560	RES, 56 OHMS 1/4W 5% C.FILM
R067	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R068	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R069	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R070	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R071	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R072	R01822	RES, 8.2K OHMS 1/4W 5% C.FILM
R073	R01822	RES, 8.2K OHMS 1/4W 5% C.FILM
R074	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R075	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R076	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R077	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R078	R05502	POT, 5K OHM TRIM
R079	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R080	R05502	POT, 5K OHM TRIM
R081	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R082	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R083	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R085	R01682	RES, 6.8K OHMS 1/4W 5% C.FILM
R086	R01182	RES, 1.8K OHMS 1/4W 5% C.FILM
R087	R01101	RES, 100 OHMS 1/4W 5% C.FILM
R088	R01152	RES, 1.5K OHMS 1/4W 5% C.FILM
R089	R21153	RES, 15K OHMS 1/4W 2% M.FILM
U001	U01496	BALANCED MOD/DEMOD, LM1496

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
U002	U00324	QUAD OP AMP, LM324
U003	U01496	BALANCED MOD/DEMOD, LM1496
U004	U00339	QUAD COMPARATOR, LM339
U005	U4LS37	QUAD 2 INPUT NAND, 74LS37
U006	U4S140	4 INPUT DRIVER, 74S140
U007	U4LS37	QUAD 2 INPUT NAND, 74LS37
U008	U4LS90	DECADE COUNTER, 74LS90
U009	U4LS90	DECADE COUNTER, 74LS90
U010	U4LS90	DECADE COUNTER, 74LS90
U011	U4S132	QUAD SCHMITT NAND, 74S132
U012	U4S140	4 INPUT DRIVER, 74S140
U013	U4LS90	DECADE COUNTER, 74LS90
U014	U4LS90	DECADE COUNTER, 74LS90
U015	U4LS37	QUAD 2 INPUT NAND, 74LS37
U016	U4LS90	DECADE COUNTER, 74LS90
U017	ULS153	DUAL 4 INPUT MULTIPLEXER, 74LS153
U018	U4LS37	QUAD 2 INPUT NAND, 74LS37
U020	U4LS90	DECADE COUNTER, 74LS90
U021	U07805	REG., 5V 1.5 AMP, TL780-05CKC
U022	U78M12	REG., +12V 0.5 AMP, 78M12CT
U023	U79M12	REG., -12V 1 AMP, 7912CKC
VR02	VR04735	ZENER DIODE, 6.2V
W001	R01000	JUMPER, 0 OHMS
W002	R01000	JUMPER, 0 OHMS
W003	R01000	JUMPER, 0 OHMS
Y001	Y00011	XTAL, 10 MHZ
A3	018700	PC BOARD ASSY DC/DC CONVERTER OPTIONS 52, 53, 54
C001	C00202	CAP 0.1 μF, 1600V, DISC CERAMIC
CR01	CR00751	DIODE, MR751
J001	J10014	HEADER, 6 PIN
J002	J10014	HEADER, 6 PIN (2)
PS01	PS00122	DC-DC CONV, 9-18V IN, 15 VDC @ 2A $\pm$5 VDC @ 2.5a (OPTION 52)
PS01	PS00110	DC-DC CONV, 18-36V IN, 15 VDC @ 2A/ $\pm$5 VDC @ 2.5A (OPTION 53)
PS01	PS00123	DC-DC CONV, 36-72V IN, 15 VDC @ 2A/ $\pm$5 VDC @ 2.5A (OPTION 54)
PS02	PS00108	DC-DC CONV, 5V IN, 12 VDC @ 500 mA
PS03	PS00109	5V IN, 15 VDC @ 100 mA

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
A3	027030	PC BOARD ASSEMBLY,DC/DC CONVERTER OPT 55
C001	C09471	CAP 470 μF, 50V LITIC
C002	C09471	CAP 470 μF, 50V LITIC
C003	C09471	CAP 470 μF, 50V LITIC
C004	C09471	CAP 470 μF, 50V LITIC
CR01	CR05059	RECTIFIER,1A,200 PIV
CR02	CR05059	RECTIFIER,1A,200 PIV
J001	J10014	HEADER, 6 PIN
J002	J10014	HEADER, 6 PIN
L001	L04000	INDUCTOR, TOROID
L002	L04000	INDUCTOR, TOROID
PS01	PS00113	DC-DC CONV, 24V IN, 15 VDC @ 540 MA
PS02	PS00113	DC-DC CONV, 24V IN, 15 VDC @ 540 MA
R001	R01752	RES, 7.5K OHMS 1/4W 5% C.FILM
A4	027040	PC BOARD ASSEMBLY, OUTPUT
C001	C26104	CAP, .1 μF 50V CERAMIC MONO
C002	C26104	CAP, .1 μF 50V CERAMIC MONO
C003	C26104	CAP, .1 μF 50V CERAMIC MONO
C004	C26104	CAP, .1 μF 50V CERAMIC MONO
C005	C26104	CAP, .1 μF 50V CERAMIC MONO
C006	C26104	CAP, .1 μF 50V CERAMIC MONO
C007	C26104	CAP, .1 μF 50V CERAMIC MONO
C008	C26104	CAP, .1 μF 50V CERAMIC MONO
C009	C26104	CAP, .1 μF 50V CERAMIC MONO
C010	C26104	CAP, .1 μF 50V CERAMIC MONO
C011	C05121	CAP, 120pF MICA
C013	C26104	CAP, .1 μF 50V CERAMIC MONO
C014	C05121	CAP, 120pF MICA
C015	C26104	CAP, .1 μF 50V CERAMIC MONO
C016	C26104	CAP, .1 μF 50V CERAMIC MONO
C017	C05121	CAP, 120pF MICA
C019	C26104	CAP, .1 μF 50V CERAMIC MONO
C020	C26104	CAP, .1 μF 50V CERAMIC MONO
C021	C26104	CAP, .1 μF 50V CERAMIC MONO
C023	C05121	CAP, 120pF MICA
C025	C26104	CAP, .1 μF 50V CERAMIC MONO
C026	C26104	CAP, .1 μF 50V CERAMIC MONO
C027	C26104	CAP, .1 μF 50V CERAMIC MONO
C028	C05121	CAP, 120pF MICA
C030	C26104	CAP, .1 μF 50V CERAMIC MONO
C031	C26104	CAP, .1 μF 50V CERAMIC MONO
C032	C26104	CAP, .1 μF 50V CERAMIC MONO

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
C035	C05121	CAP, 120pF MICA
C036	C26104	CAP, .1 μF 50V CERAMIC MONO
C037	C26104	CAP, .1 μF 50V CERAMIC MONO
C038	C26104	CAP, .1 μF 50V CERAMIC MONO
C039	C05121	CAP, 120pF MICA
C040	C05121	CAP, 120pF MICA
C041	C05121	CAP, 120pF MICA
C042	C05121	CAP, 120pF MICA
C043	C26104	CAP, .1 μF 50V CERAMIC MONO
C044	C09010	CAP, 1.0 μF 50V LITIC
C048	C09010	CAP, 1.0 μF 50V LITIC
C049	C26104	CAP, .1 μF 50V CERAMIC MONO
C050	C26104	CAP, .1 μF 50V CERAMIC MONO
C051	C26104	CAP, .1 μF 50V CERAMIC MONO
C052	C26104	CAP, .1 μF 50V CERAMIC MONO
C053	C26104	CAP, .1 μF 50V CERAMIC MONO
C054	C26104	CAP, .1 μF 50V CERAMIC MONO
C055	C26104	CAP, .1 μF 50V CERAMIC MONO
C056	C26104	CAP, .1 μF 50V CERAMIC MONO
C057	C26104	CAP, .1 μF 50V CERAMIC MONO
CR02	CR00277	DIODE, IN277
CR03	CR00277	DIODE, IN277
CR04	CR00277	DIODE, IN277
CR06	CR00277	DIODE, IN277
CR07	CR00277	DIODE, IN277
CR08	CR00277	DIODE, IN277
CR10	CR00277	DIODE, IN277
CR11	CR00277	DIODE, IN277
CR12	CR00277	DIODE, IN277
CR14	CR00277	DIODE, IN277
CR15	CR00277	DIODE, IN277
CR16	CR00277	DIODE, IN277
CR18	CR00277	DIODE, IN277
CR19	CR00277	DIODE, IN277
CR20	CR00277	DIODE, IN277
CR21	CR05059	RECTIFIER,1A,200 PIV
CR22	CR05059	RECTIFIER,1A,200 PIV
J001	J02006	HEADER, 6 PIN (2)
J002	J02006	HEADER, 6 PIN
J003	J02006	HEADER, 6 PIN (2)
J004	J13107	SOCKET, 7 PIN PC MOUNT
K001	K00002	RELAY, DP DT
K002	K00002	RELAY, DP DT
L001	L023R9	CHOKE, 3.9 UH
L002	L023R9	CHOKE, 3.9 UH
L003	L023R9	CHOKE, 3.9 UH
L004	L023R9	CHOKE, 3.9 UH
L005	L023R9	CHOKE, 3.9 UH

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
L006	L023R9	CHOKE, 3.9 UH
L007	L023R9	CHOKE, 3.9 UH
L008	L023R9	CHOKE, 3.9 UH
L009	L04000	INDUCTOR, TOROID
L010	L04000	INDUCTOR, TOROID
L011	L04000	INDUCTOR, TOROID
L012	L04000	INDUCTOR, TOROID
L013	L023R9	CHOKE, 3.9 UH
L014	L023R9	CHOKE, 3.9 UH
L015	L04000	INDUCTOR, TOROID
L016	L04000	INDUCTOR, TOROID
Q001	Q0VN10	J-FET N-CHANNEL, VN10KM
Q002	Q0VN10	J-FET N-CHANNEL, VN10KM
R001	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R002	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R003	R01202	RES, 2K OHMS 1/4W 5% C.FILM
R004	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R005	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R006	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R007	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R008	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R009	R01121	RES, 120 OHMS 1/4W 5% C.FILM
R012	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R013	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R014	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R015	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R016	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R017	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R018	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R019	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R020	R01390	RES, 39 OHMS 1/4W 5% C.FILM
R021	R01104	RES, 100K OHMS 1/4W 5% C.FILM
R022	R01270	RES, 27 OHMS 1/4W 5% C.FILM
R023	R01270	RES, 27 OHMS 1/4W 5% C.FILM
R024	R01270	RES, 27 OHMS 1/4W 5% C.FILM
R025	R01121	RES, 120 OHMS 1/4W 5% C.FILM
R026	R01101	RES, 100 OHMS 1/4W 5% C.FILM
SW01	S00340	SWITCH, 1 POS DIP
U002	U75141	DUAL LINE RECEIVER, 75141
U003	ULS490	DUAL 4-BIT DECADE COUNTER, 74LS490
U004	UAS804	HEX NAND DRIVER, 74AS804
U005	UAS804	HEX NAND DRIVER, 74AS804
U006	U00339	QUAD COMPARATOR, LM339
U007	U00339	QUAD COMPARATOR, LM339
U008	U78M12	REGULATOR, +12V 0.5 AMP, 78M12CT
U008	U78T12	REGULATOR, +12V 3.0 AMP, 78T12CT

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
U009	U4LS37	QUAD 2 INPUT NAND, 74LS37
U010	U75179	RS-422A DRIVER/RECEIVER, 75179
U011	U75179	RS-422A DRIVER/RECEIVER, 75179
A5	002500	PC BOARD ASSY, OSC/PWR SUPPLY
C001	C12226	CAP, 22 μF 15V TANT
C004	C15685	CAP, 6.8 μF 35V TANT
C005	C12226	CAP, 22 μF 15V TANT
C006	C22105	CAP, 1 μF 100V POLYESTER
C007	C02103	CAP, .01 μF 25V DISC CERAMIC
C008	C09471	CAP, 470 μF 50V LITIC
C009	C09471	CAP, 470 μF 50V LITIC
C010	C15685	CAP, 6.8 μF 35V TANT
C011	C05102	CAP, 1000pF MICA
CR01	CR05059	RECTIFIER,1A,200 PIV
CR02	CR05059	RECTIFIER,1A,200 PIV
CR03	CR05059	RECTIFIER,1A,200 PIV
CR04	CR05059	RECTIFIER,1A,200 PIV
CR05	CR04148	DIODE, IN4148
CR06	CR05059	RECTIFIER,1A,200 PIV
CR07	CR05059	RECTIFIER,1A,200 PIV
CR08	CR04148	DIODE, IN4148
J001	J10014	HEADER, 6 PIN
J002	J10014	HEADER, 6 PIN (2)
Q002	Q04126	TRANSISTOR, PNP, 2N4126
Q003	Q04124	TRANSISTOR, NPN, 2N4124
Q004	Q00L51	TRANSISTOR, PNP, MPS-L51
Q005	Q04126	TRANSISTOR, PNP, 2N4126
Q006	Q00L51	TRANSISTOR, PNP, MPS-L51
Q007	Q04126	TRANSISTOR, PNP, 2N4126
Q008	Q04124	TRANSISTOR, NPN, 2N4124
Q009	Q00034	TRANSISTOR, PNP, TIP34A
Q010	Q00033	TRANSISTOR, NPN, TIP33A
R004	R07203	POT, 20K OHM 18 TURN TRIM
R005	R11363	RES, 36K OHMS 1/4W 5% M.FILM
R006	R21823	RES, 82 K OHMS 1/4W 2% M.FILM
R009	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R010	R01182	RES, 1.8K OHMS 1/4W 5% C.FILM
R011	R01333	RES, 33K OHMS 1/4W 5% C.FILM
R012	R01393	RES, 39K OHMS 1/4W 5% C.FILM
R013	R03182	RES, 1.8K OHMS 1W 5% C.COMP
R014	R022R4	RES, 2.4 OHMS 1/2W 5% C.FILM
R015	R01273	RES, 27K OHMS 1/4W 5% C.FILM
R016	R01273	RES, 27K OHMS 1/4W 5% C.FILM
R017	R01222	RES, 2.2K OHMS 1/4W 5% C.FILM

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
R018	R05103	POT, 10K OHM TRIM
R019	R01272	RES, 2.7K OHMS 1/4W 5% C.FILM
R020	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R021	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R022	R11123	RES, 12K OHMS 1/4W 5% M.FILM
R023	R03182	RES, 1.8K OHMS 1W 5% C.COMP
R024	R01470	RES, 47 OHMS 1/4W 5% C.FILM
R025	R05102	POT, 1K OHM TRIM
R026	R21562	RES, 5.6K OHMS 1/4W 2% M.FILM
R027	R11392	RES, 3.9K OHMS 1/4W 5% M.FILM
R028	R01102	RES, 1 K OHMS 1/4W 5% C.FILM
R030	R01101	RES, 100 OHMS 1/4W 5% C.FILM
U001	002590	OSCILLATOR
U002	U00723	VOLTAGE REGULATOR, 723
VR01	VR05242	ZENER DIODE, 12V
W001	R01000	JUMPER, 0 OHMS
W002	R01000	JUMPER, 0 OHMS
W003	R01000	JUMPER, 0 OHMS
A6	018100	PC BOARD ASSEMBLY, FTC
C001	C26104	CAP, .1 μF 50V CERAMIC MONO
C002	C26104	CAP, .1 μF 50V CERAMIC MONO
C003	C26104	CAP, .1 μF 50V CERAMIC MONO
C004	C26104	CAP, .1 μF 50V CERAMIC MONO
C005	C26104	CAP, .1 μF 50V CERAMIC MONO
C006	C26104	CAP, .1 μF 50V CERAMIC MONO
C007	C26104	CAP, .1 μF 50V CERAMIC MONO
C008	C26104	CAP, .1 μF 50V CERAMIC MONO
C009	C26104	CAP, .1 μF 50V CERAMIC MONO
C010	C26104	CAP, .1 μF 50V CERAMIC MONO
C011	C26104	CAP, .1 μF 50V CERAMIC MONO
C012	C26104	CAP, .1 μF 50V CERAMIC MONO
C013	C26104	CAP, .1 μF 50V CERAMIC MONO
C016	C05150	CAP, 15pF MICA
C017	C05100	CAP, 10pF MICA
C018	C26104	CAP, .1 μF 50V CERAMIC MONO
C019	C26104	CAP, .1 μF 50V CERAMIC MONO
C020	C26104	CAP, .1 μF 50V CERAMIC MONO
C021	C09010	CAP, 1.0 μF 50V LITIC
C022	C05500	CAP, 50pF MICA
C024	C07220	CAP, 22 μF 25V LITIC
C025	C26104	CAP, .1 μF 50V CERAMIC MONO
C026	C26104	CAP, .1 μF 50V CERAMIC MONO
C027	C26104	CAP, .1 μF 50V CERAMIC MONO
C028	C05101	CAP, 100pF MICA
C029	C26104	CAP, .1 μF 50V CERAMIC MONO
C030	C26104	CAP, .1 μF 50V CERAMIC MONO

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
C031	C26104	CAP, .1 μF 50V CERAMIC MONO
C032	C05101	CAP, 100pF MICA
C033	C26104	CAP, .1 μF 50V CERAMIC MONO
J001	J02006	HEADER, 6 PIN (2)
J002	J02006	HEADER, 6 PIN
J003	J02006	HEADER, 6 PIN
J004	J02006	HEADER, 6 PIN
J005	J02006	HEADER, 6 PIN (2)
R001	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R002	R07203	POT, 20K OHM 18 TURN TRIM
R008	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R009	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R010	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R011	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R012	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R013	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R014	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R015	R01154	RES, 150K OHMS 1/4W 5% C.FILM
R017	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R018	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R019	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R020	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R021	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R022	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R023	R01151	RES, 150 OHMS 1/4W 5% C.FILM
R024	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R025	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R029	R01121	RES, 120 OHMS 1/4W 5% C.FILM
R030	R01471	RES, 470 OHMS 1/4W 5% C.FILM
R031	R01103	RES, 10K OHMS 1/4W 5% C.FILM
R032	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R033	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
R034	R01472	RES, 4.7K OHMS 1/4W 5% C.FILM
RP01	R36103	RES NETWORK 10K OHM SIP
RP02	R36103	RES NETWORK 10K OHM SIP
U001	S00336	SWITCH, 8 POS DIP
U002	U08254	PROGRAM INTERVAL TIMER, 8254
U003	U08254	PROGRAM INTERVAL TIMER, 8254
U004	U82542	PROGRAM INTERVAL TIMER, 8254-2
U005	U01220	2K X 8 RAM, DS1220AB
U006	EP0008	EPROM, FTC 3.32, 2764A, OPT56
U006	EP0013	EPROM, FTC 3.22, 2764A, STD
U006	EP0014	EPROM, FTC 3.12, 2764A, OPT31
U007	U08255	PROGRAMMABLE INTERFACE, 8255A-5
U008	ULS138	3 INPUT MULTIPLEXER, 74LS138
U009	U4LS86	QUAD EXCLUSIVE OR, 74LS86
U010	ULS109	DUAL J-K F/F, 74LS109A

REPLACEABLE PARTS - PC BOARD ASSEMBLY

REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION
U011	ULS158	QUAD 2 INPUT MULTIPLEXER, 74LS158
U012	ULS373	OCTAL D-LATCH, 74LS373
U013	U08031	8-BIT MICROCOMPUTER, P8031
U014	U07417	HEX O.C. BUFFER, 7417
U015	U00411	OP AMP/LOW OFFSET, LF411
U016	U01230	12 BIT D/A, DAC1230
U018	S00336	SWITCH, 8 POS DIP
U019	U00324	QUAD OP AMP, LM324
U020	U4LS14	HEX SCHMITT INVERTER, 74LS14
U021	U07417	HEX O.C. BUFFER, 7417
U022	ULS109	DUAL J-K F/F, 74LS109A
U023	U01488	QUAD LINE DRIVER, 1488
U024	ULS109	DUAL J-K F/F, 74LS109A
U025	ULS109	DUAL J-K F/F, 74LS109A
U026	U6LS31	QUAD RS422 DRIVER, 26LS31
U027	U01489	QUAD LINE RECEIVER, 1489
U028	U01232	POWER MONITOR, DS1232
W001	R01000	JUMPER, 0 OHMS
W002	R01000	JUMPER, 0 OHMS

ANCILLARY KIT

Y001	Y00014	XTAL, 11.059 MHZ
0001	W01000	LINE CORD
0002	P13007	TERM BLOCK, 7 POS
0003	P01115	PLUG, 15 PIN MOLEX
0004	P01100	PIN, MOLEX CRIMP (TOTAL 15 PINS)
0005	004490	TERMINATOR, 50 OHM, DC ISOLATED (TOTAL 5, OPT 3)
0012	P00002	PLUG, BNC, UG-88/U
0013	MAN8165	MANUAL 8165
F001	F00R75	FUSE, 3/4A, 3AG
F001	F001R2	FUSE, 1-1/4A, 3AG, OPT 03
F002	F001R0	FUSE, 1.0A, 3AG Opt 55
F002	F00R38	FUSE, 3/8A, 3AG

MANUAL ERRATA

MANUAL 8165 MANUAL ERRATA

This section contains manual corrections or changes made to the instrument after the last printing of the manual.

PRODUCT ENHANCEMENT NOTICE

INTRODUCTION

Test points to measure the receiver AGC voltage and VCO voltage are now provided on the Model 8165 Rear Panel. This change eliminates the need to partially disassemble the instrument when troubleshooting or aligning the Model 8206A Antenna.

CUT-IN POINT

This change is included in all units with serial numbers 8165-0897 and above.

DESCRIPTION

The AGC and VCO test points are now located on the **AUX IN/OUT** connector. The WWVB phase lock 10 MHz, time code, and lock indication signals have been removed from this connector to make room for the test points. These signals were used to synchronize the Model 8171A Clock, now obsolete.

The AGC voltage indicates the received signal strength of the WWVB transmission. The higher the AGC voltage, the greater the signal received. The Model 8165 receiver operates over an AGC range of 1.0 VDC minimum lock threshold to a maximum of 3.6 VDC. The signal strength measurement is especially useful when selecting an antenna location or when orienting the directional Model 8206A Loop Antenna. Select the antenna site or antenna direction that produces the highest AGC voltage. To measure the AGC voltage, connect the negative probe of a DMM to PIN 10 and the positive probe to PIN 13 of the **AUX IN/OUT** connector.

The VCO test point measures the voltage applied to the WWVB phase locked voltage-controlled crystal oscillator. The VCO test point is located on PIN 14 of the **AUX IN/OUT** connector. PIN 15 is the DMM ground connector. The VCO voltage changes to compensate for crystal aging, and may eventually require retuning the crystal to re-center the control voltage.

The receiver can maintain phase lock to WWVB whenever the VCO voltage falls within the range of 0.9 to 1.9 VDC. The VCO test point should be periodically checked to verify that the control voltage is within this range. If the VCO voltage falls outside of these limits, the control voltage may not have sufficient pull-in to stay locked

to WWVB. When a receiver has insufficient pull-in range, it may experience intermittent lock or loss of lock during the diurnal periods.

VCO ADJUSTMENT PROCEDURE

Follow the procedure described below if it is necessary to adjust the VCO. Tools required are a Phillips screwdriver, a multimeter, and a flat bladed non-metallic tuning tool.

FOR BEST RESULTS:
Perform this adjustment only after the unit has reached operational temperature and under the same ambient temperature conditions normally found.

Select a day when the weather is generally clear. Poor atmospheric conditions increase the control voltage variations, making the final VCO adjustment difficult.

The antenna must be connected and in good working order to make this adjustment.

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1. Remove the top cover.

2. Remove the two (2) Phillips head screws that secure the FTC board.

3. Tilt the FTC board back to access the receiver board assembly.

4. Set the DMM to read DC volts. Insert the positive probe into PIN 14 of the **AUX IN/OUT** connector. Insert the negative lead into PIN 15.

5. Refer to the receiver assembly drawing on Page 4-11 of the 8165 manual to locate trimmer capacitor C10. Carefully adjust C10 in small increments to produce a VCO voltage of 1.4 $\pm$.1 VDC. Allow the VCO voltage to stabilize between adjustments of the trimmer capacitor.

6. Adjustment is complete. Reassemble the unit and return it to service.

MANUAL CHANGES

Incorporate the following changes into the Model 8165 Instruction Manual.

1. Time code outputs are no longer provided on the Model 8165. Delete **Section 2.3 Time Code Outputs** from the manual.

2. Replace Paragraph 3 of **Section 2.4 Signal Strength** with the following:

   To measure the AGC voltage, place the positive lead of a DC voltmeter into PIN 13 and the negative lead into PIN 10 of the Rear Panel AUX IN/OUT connector. The voltage is approximately 2.0 VDC at a field strength of 100 μV per meter using a Model 8208 Whip Antenna or a properly oriented Model 8206A Loop Antenna. The AGC voltage will increase in strong signal locations, rising to a limiting value of approximately +3.6 volts as the front end input increases.

3. Replace the description of the **AUX IN/OUT** connector Section 2.6.4 with the following:

   ### *2.6.4 AUX IN/OUT (J8)*

   Auxiliary and remote functions of the receiver are available at this 15-pin connector. Use Figure 2-4, AUX IN/OUT (J8) VIEWED FROM THE REAR OF THE UNIT, to locate the pins. The mating connector and pins are furnished in the Ancillary Kit.

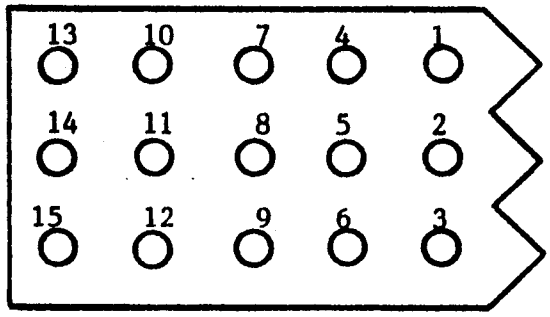

FIGURE 2-4 AUX IN/OUT (J8), VIEWED FROM THE REAR OF THE UNIT

PIN 1 - (+) MINOR ALARM - This lead is positive relative to PIN 2 when the function is asserted. The Minor Alarm is asserted whenever an Output Fault or Adjust Oscillator Alarm occurs. Twisted pair should be used for PIN 1 and PIN 2.

PIN 2 - (-) MINOR ALARM - This lead is negative relative to PIN 1 when the function is asserted.

PIN 3 - EXTERNAL BATTERY INPUT - For continuous oven and oscillator operation in the event of power failure, an external battery can be connected here. The battery will be float-charged whenever line power is on. The maximum charge rate is 250 mA. Recommended battery type is sealed lead-acid, 24 VDC, 1-2 A-H or greater capacity. The **OVEN DC** switch must be in the EXT position.

PIN 6 - EXTERNAL BATTERY INPUT GROUND

PIN 8 - (+) MAJOR ALARM - This lead is positive relative to PIN 9 when the function is asserted. A twisted pair should be used for PINs 8 and 9. The signal returns to normal when the alarm condition is cleared. A Major Alarm is asserted whenever the CPU, Signal or Frequency alarms occur.

PIN 9 - (-) MAJOR ALARM - This lead is negative relative to PIN 8 when the function is asserted. The signal returns to normal when the alarm condition is cleared.

PIN 10 - (-) AGC TEST POINT - Connect the negative lead of a DMM here to measure the receiver AGC voltage or signal strength.

PIN 11 - EXTERNAL PHASE METER - This output may be used to operate a 0-1 mA meter or chart recorder to compare the phase relationship between the frequency standard and the NIST phase- locked signal. Full scale represents 50 microseconds of relative time.

PIN 12 - EXTERNAL METER GROUND

PIN 13 - (+) AGC TEST POINT - Connect the positive lead of a DMM here to measure the receiver AGC voltage or signal strength.

PIN 14 - VCO TEST POINT - This test point measures the control voltage applied to the WWVB phase locked VCO. The VCO voltage should fall between 1.0 and 1.8 VDC to ensure proper operation.

PIN 15 - VCO TEST POINT GROUND

4. Delete Paragraphs **3.2.1 Time Code**, **3.2.2 Lock Status**, and **3.2.3 10-MHz Output** from **SECTION 3.2 RECEIVER OUTPUTS.** These signals are no longer available from the Model 8165.